M02066

3.3 Volt Laser Driver IC for Applications to 3 Gbps Data Sheet

The M02066 is a highly integrated, programmable laser driver intended for SONET/SDH applications with FEC to 3 Gbps. Using differential PECL data and clock inputs, the M02066 supplies the bias and modulation current required to drive an edge-emitting laser. The modulation output can be DC-coupled to the laser diode, giving a significant power saving over AC-coupled operation.

The M02066 includes automatic power control to maintain a constant average laser output power over temperature and life. In addition, the modulation current can be temperature compensated to minimize variation in extinction ratio over temperature.

Output flags indicate laser end of life as well as failure of the APC circuitry to maintain average output power.

General Note: This product was previously called the CX02066.

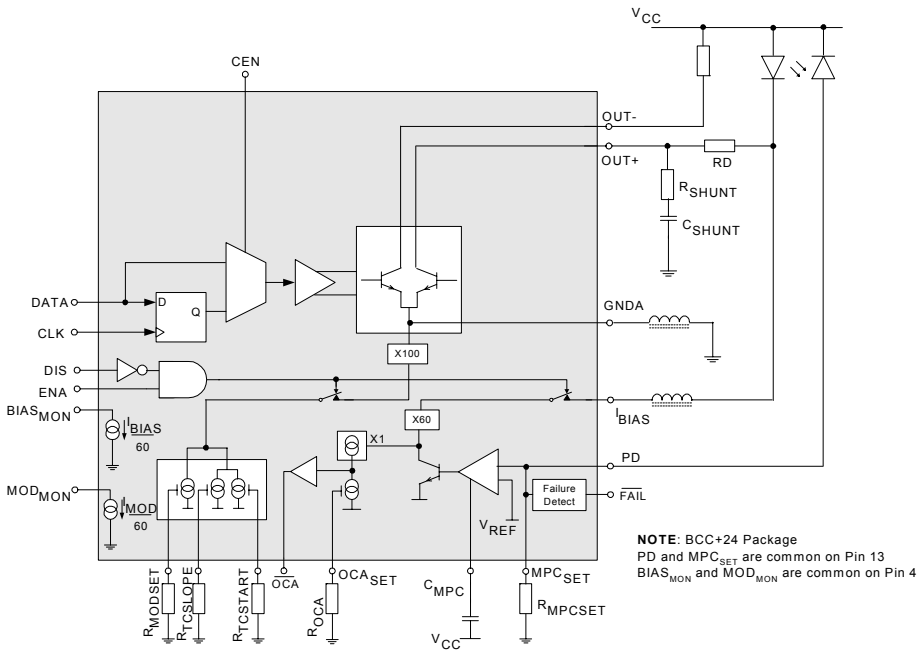
Features

- High speed operation; suitable for applications to 3 Gbps.
- Typical rise/fall times of 90 ps.
- DC or AC coupled modulation drive.
- Differential data and clock inputs to minimize pattern dependent jitter.
- Independently Programmable Laser Bias and Modulation currents.
- Bias current to 100 mA and modulation current to 85 mA at VCC = 3.3 V
- Automatic Laser Power Control, with programmable temperature compensation and 'Slow-Start'.
- Bias and modulation current monitor
- Operates with +3.3 Volt supply
- Functionally compatible with MAX 3869
- The M02066-21 and M02066-51 are available in a BCC+24 package. The M02066-82 is available in a TQFP32 package.
- Available in RoHS compliant packages

Applications

- Short reach and Metro SONET/SDH
- Datacomms Modules
- Add/Drop Multiplexers
- Digital Cross Connects

Functional Block Diagram



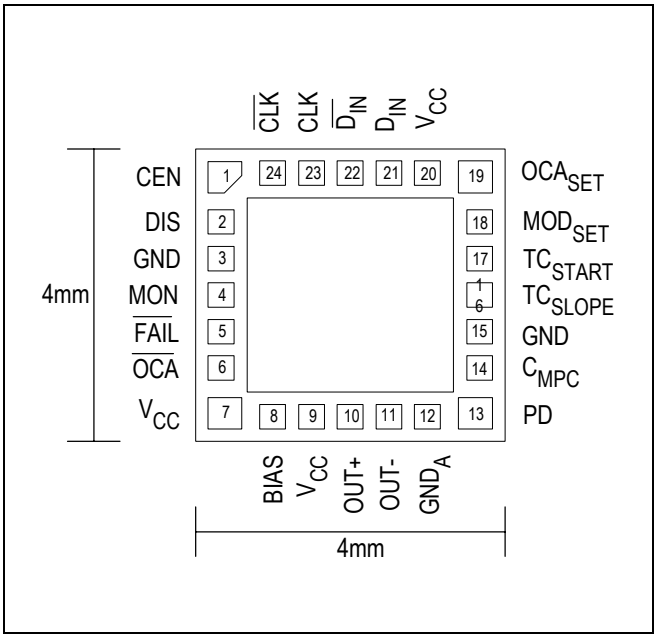
Ordering Information

Part Number	Package
M02066-21	BCC+24 package with 20 ps or less DCD
M02066-51	BCC+24 package with 50 ps or less DCD
M02066-82	TQFP32 package with 80 ps or less DCD
M02066-EVME	BCC+24 electrical evaluation board
M02066-T-EVM	Optical evaluation board, TO-can laser
M02066G-21 *	BCC+24 RoHS compliant package, with 20 ps or less DCD
M02066G-51 *	BCC+24 RoHS compliant package, with 50 ps or less DCD
M02066G-82 *	TQFP32 RoHS compliant package, with 80 ps or less DCD
* The letter “G” designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.	

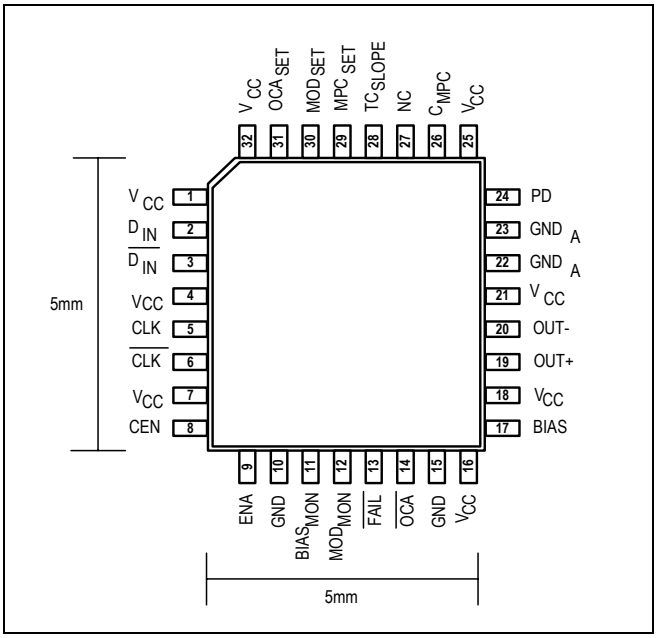
Revision History

Revision	Level	Date	ASIC Revision	Description
D	Preliminary	November 2006	x	Added RoHS package information, updated format, no specification changes.

BCC+24L Top View



TQFP32 Top View



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Functional operation at these levels is not implied.

Table 1-1. Absolute Maximum Ratings

Parameter	Rating	Units
Power supply (V_{CC}-GND)	-0.5 to +6.0	V
Operating ambient	-40 to +85	°C
Storage temperature	-65 to +150	°C
Maximum laser bias current	120	mA
Maximum laser modulation current (through OUT+/OUT2+, OUT-/OUT2-)	100	mA

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply (V_{CC}-GND)	3.3 ± 10%	V
Junction temperature (die)	-40 to + 120	°C
Operating ambient	-40 to + 85	°C

1.3 DC Characteristics

V_{CC}=+3.3V ± 10%, T_A=-40 °C to +85 °C, unless otherwise noted.

Table 1-3. DC Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Supply current	I_{BIAS} = 50 mA I_{MOD} = 50 mA Excluding I_{BIAS} and I_{MOD}	-	57	-	mA
Supply current	I_{BIAS} = 100 mA I_{MOD} = 85 mA Excluding I_{BIAS} and I_{MOD}	-	70	75	mA
Bias current adjust range	Limited by OCA_{SET} across temperature range	2	-	100	mA
Bias current with output disabled	Tx_Disable = HIGH	-	-	300	µA
Maximum bias current limit	T_A = +85 °C (adjustable)	100(1)	-	-	mA
Change in OCA_{SET} over temperature		-	200	-	µA/°C
Monitor diode reverse bias voltage		-	2.1	-	V
Monitor diode current adjustment range		10	-	1500	µA
TTL/CMOS input HIGH voltage (CEN, DIS)		2.0	-	-	V
TTL/CMOS input LOW voltage (CEN, DIS)		-	-	0.8	V
CMOS output HIGH voltage ($\overline{FAIL}$, $\overline{OCA}$)		2.4	-	-	V
CMOS output LOW voltage ($\overline{FAIL}$, $\overline{OCA}$)		-	-	0.4	V
Differential input impedance	Data and clock inputs	2.5	-	-	kΩ
Common-mode input voltage		V_{CC}-1.7		V_{CC}-(V_{IN}(Diff)/4)	V
Self-biased common mode input voltage	Data and clock inputs	V_{CC}-1.7	-	V_{CC}-0.47	V

NOTE:

(V_{CC} = +3.3 V ±10%, T_A = 40 °C to + 85 °C, unless otherwise noted)

1. R_{OCASET} = 0 Ω

1.4 AC Characteristics

VCC = +3.3V ±10%, TA = -40 °C to +85 °C, unless otherwise noted.

Table 1-4. AC Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units.
Differential input voltage	= 2 x ($D_{IN\ HIGH}$ - $D_{IN\ LOW}$) (clock inputs follow same relationship)	300	—	1860	mV
Modulation current range		2.5	—	85	mA
Modulation current with output disabled	DIS=HIGH	—	—	300	µA
Programmable range for modulation current temperature coefficient	Adjustable	500	—	10^4	ppm/°C
Programmable temperature at which modulation current TC compensation enables	Programmed by choice of R_{TCSET}	20	—	60	°C
Modulation output rise time Modulation output fall time	20% to 80% into 25 Ω *(1)* 20% to 80% into 25 Ω	— —	90 90	— —	ps
Overshoot of modulation output current	Into 25 Ω load	-10	—	+10	%
Modulation output pulse width distortion	Measured using alternating 1-0 pattern RMODSET = 7 kΩ			20*(2)*	ps
Modulation output pulse width distortion	Measured using alternating 1-0 pattern RMODSET = 7 kΩ			50*(3)*	ps
Modulation output pulse width distortion	Measured using alternating 1-0 patternRMODSET = 7 kΩ			80*(4)*	ps
Modulation output random jitter	rms 12 kHz to 20 MHz	—	—	4	mUI
Total output jitter (data input latch enabled)	Peak-to-peak. Measured into 25 Ω load using 1867 MHz Bessel filter: 2^{23}-1 PRBS at 2.488 Gbps; using clock inputs (includes PWD, random and deterministic)	—	—	42*(2)*	ps
Total output jitter (data input latch enabled)	Peak-to-peak. Measured into 25 Ω load using 1867 MHz Bessel filter: 2^{23}-1 PRBS at 2.488 Gbps; using clock inputs (includes PWD, random and deterministic)	—	—	72*(3)*	ps
Total output jitter (data input latch enabled)	Peak-to-peak. Measured into 25 Ω load using 1867 MHz Bessel filter: 2^{23}-1 PRBS at 2.488 Gbps; using clock inputs (includes PWD, random and deterministic)	—	—	100*(4)*	ps

NOTES:

(V_{CC} = +3.3 V ±10%, T_A = 40 °C to + 85 °C, unless otherwise noted)

1. I_{MOD} = 28 mA
2. Applies only to the M02066-21.
3. Applies only to the M02066-51.
4. Applies only to the M02066-82.

2.0 Pin Description

2.1 Pin Descriptions

Table 2-1. Pin Descriptions (BCC+24)

Pin No.	Name	Function
1	CEN	Clock enable input (TTL/CMOS). Set HIGH or not connected to use CLK inputs, LOW when not using CLK inputs
2	DIS	Bias and modulation output disable (TTL/CMOS). LOW for normal operation
3	GND	Ground
4	MON	Monitor output, connect a resistor between this pin and V_{CC} to monitor the sum of bias and modulation currents
5	FAIL	Mean power control failure indicator (TTL/CMOS). Goes LOW when control loop is no longer able to maintain constant current at PD
6	OCA	Over-current alarm (TTL/CMOS). Goes LOW when I_{BIAS} exceeds the preset bias current limit
7	V_{CC}	Power supply
8	BIAS	Laser bias current output
9	V_{CC}	Power supply
10	OUT+	Positive modulation current output. Sinks current when D_{IN} is HIGH
11	OUT-	Negative modulation current output. Sinks current when $\overline{D}_{IN}$ is HIGH
12	GND_A	Ground for output stage. (inductor to ground)
13	PD	Monitor photo diode input. This input is connected to the monitor photodiode anode for automatic power control. A resistor between this pin and ground sets the mean optical power
14	C_{MPC}	Mean power control loop dominant pole capacitor
15	GND	Ground
16	TC_{SLOPE}	Connecting a resistor between this pin and ground sets the temperature coefficient of I_{MODSET} (using the internal IC temperature)
17	TC_{START}	Secondary temperature coefficient of I_{MOD}. A resistor on this pin to ground sets the temperature at which the temperature compensation starts
18	MOD_{SET}	Modulation current set. Connect a resistor between this pin and ground to set
19	OCA_{SET}	Over current alarm set. Connect a resistor between this pin and ground to set
20	V_{CC}	Power supply
21	D_{IN}	Positive data input (PECL). Self biased

Table 2-1. Pin Descriptions (BCC+24) (Continued)

Pin No.	Name	Function
22	$\overline{D}_{IN}$	Negative data input (PECL). Self biased
23	CLK	Positive clock input (PECL). Self biased. Connect to V_{cc} if not used
24	CLK	Negative clock input (PECL). Self biased. Can be disconnected if not used
NOTE: The center pad must be connected to ground through an array of vias for good electrical and thermal performance.		

Table 2-2. Pin Descriptions (TQFP 32)

Pin No.	Name	Function
1, 4, 7, 16, 18, 21, 25, 32	V_{CC}	Power supply
2	D_{IN}	Positive data input (PECL). Self biased
3	$\overline{D}_{IN}$	Negative data input (PECL). Self biased
5	CLK	Positive clock input (PECL). Self biased. Connect to V_{cc} if not used
6	$\overline{CLK}$	Negative clock input (PECL). Self biased. Can be disconnected if not used
8	CEN	Clock enable input (TTL/CMOS). Set HIGH or not connected to use CLK inputs, LOW when not using CLK inputs
9	ENA	Bias and modulation output enable (TTL/CMOS). HIGH for normal operation
10	GND	Ground
11	$BIAS_{MON}$	Bias monitor and temperature- dependent bias current limit. Connect a resistor between this pin and V_{CC} to monitor
12	MOD_{MON}	Modulation current monitor. Connect a resistor between this pin and V_{CC} to monitor
13	$\overline{FAIL}$	Mean power control failure indicator (TTL/CMOS). Goes LOW when control loop is no longer able to maintain constant current at I_{PIN}
14	$\overline{OCA}$	Over-current alarm (TTL/CMOS). Goes LOW when I_{BIAS} exceeds the preset bias current limit
15	GND	Ground
17	BIAS	Laser bias current output
19	OUT+	Positive modulation current output. Sinks current when D_{IN} is HIGH
20	OUT-	Negative modulation current output. Sinks current when $\overline{D}_{IN}$ is HIGH
22	GND_A	Ground for output stage (inductor to ground)
23	GND_A	Ground for output stage (inductor to ground)
24	PD	Monitor photo diode input. This input is connected to the monitor photodiode anode for automatic power control.
26	C_{MPC}	Mean power control dominant pole capacitor

Table 2-2. Pin Descriptions (TQFP 32) (Continued)

Pin No.	Name	Function
27	NC	Not connected and may be grounded for compatibility with MAX3869
28	TC_{SLOPE}	Connecting a resistor between this pin and ground sets the temperature coefficient of I_{MODSET} (using the internal IC temperature)
29	MPC_{SET}	A resistor between this pin and ground sets the mean optical power
30	MOD_{SET}	Modulation current set. Connect a resistor between this pin and ground to set
31	OCA_{SET}	Over current alarm set. Connect a resistor between this pin and ground to set

NOTE:

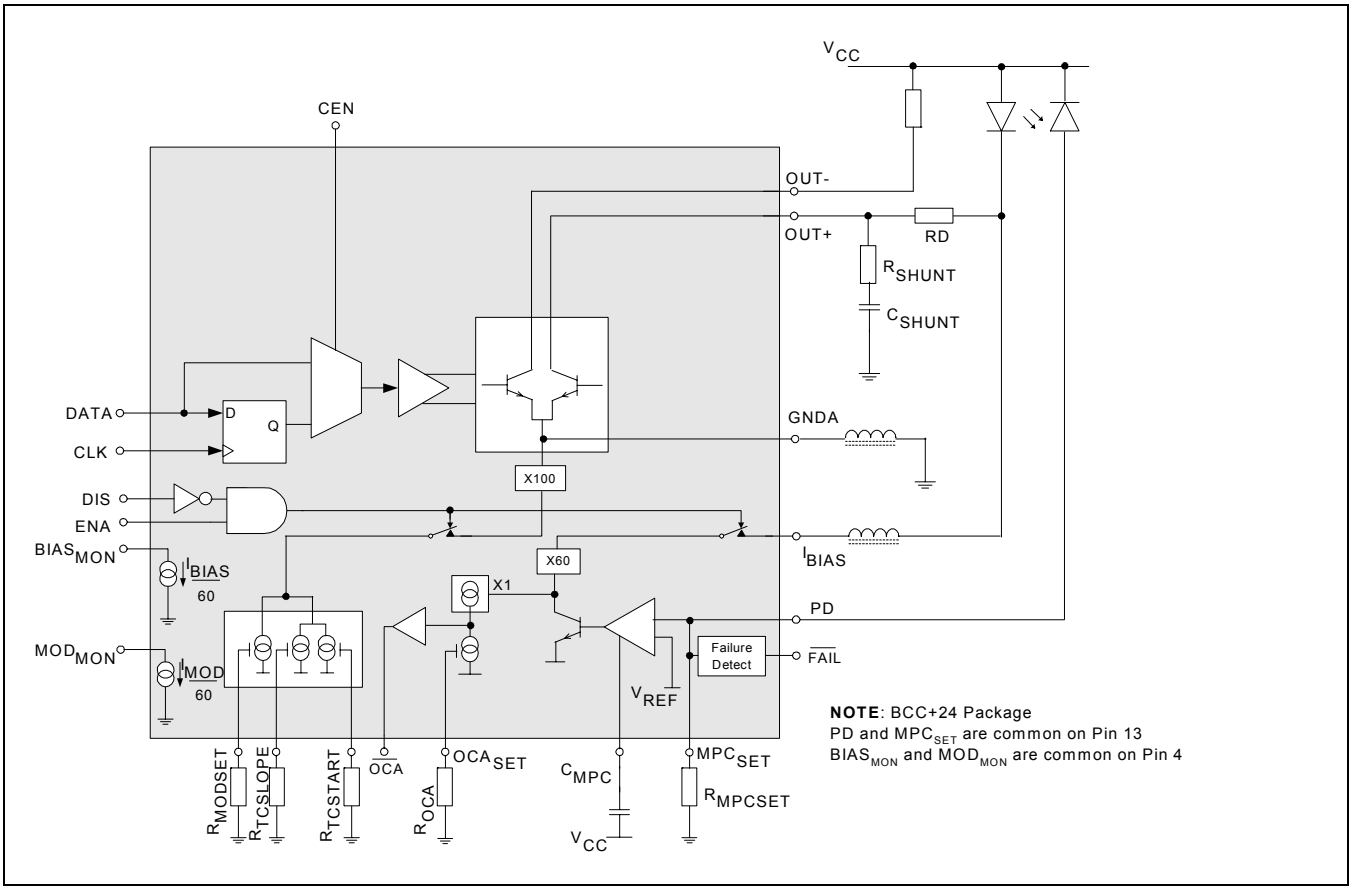
TC_{START} is internally connected to 0 V in the TQFP32.
The center pad must be connected to ground through an array of vias for good electrical and thermal performance.

3.0 Functional Description

3.1 Overview

The M02066 laser driver consists of a high-speed modulation driver and a laser bias generator with mean power control (MPC). It is optimized for high speed, low power operation at 3.3V supply. To minimize the pattern-dependent jitter of the input signal, the device accepts an input clock signal for data retiming. This feature can be enabled using the external CEN pin.

Figure 3-1. CX02068 Block Diagram



3.2 Features

- High speed operation; suitable for applications to 3 Gbps.
- Typical rise/fall times of 90 ps.
- DC or AC coupled modulation drive.
- Differential data and clock inputs to minimize pattern dependent jitter.
- Independently Programmable Laser Bias and Modulation currents.
- Bias current to 100 mA and modulation current to 85 mA at VCC = 3.3 V
- Automatic Laser Power Control, with programmable temperature compensation and ‘Slow-Start’.
- Bias and modulation current monitor
- Operates with +3.3 Volt supply
- Functionally compatible with MAX 3869
- The M02066-21 and M02066-51 are available in a BCC+24 package. The M02066-82 is available in a TQFP32 package.
- Available in RoHS compliant packages

3.3 Modulator

The M02066 modulation output is optimized for driving a 25Ω load; the minimum required voltage at OUT+ and OUT- is 0.6V. To interface with the laser diode, a matching resistor (RD) is required for impedance matching. An RC shunt network is necessary to compensate for the laser diode parasitic inductance, thereby improving the optical eye.

Typical values are R_{SHUNT} = 39Ω, C_{SHUNT} = 3.9 pF.

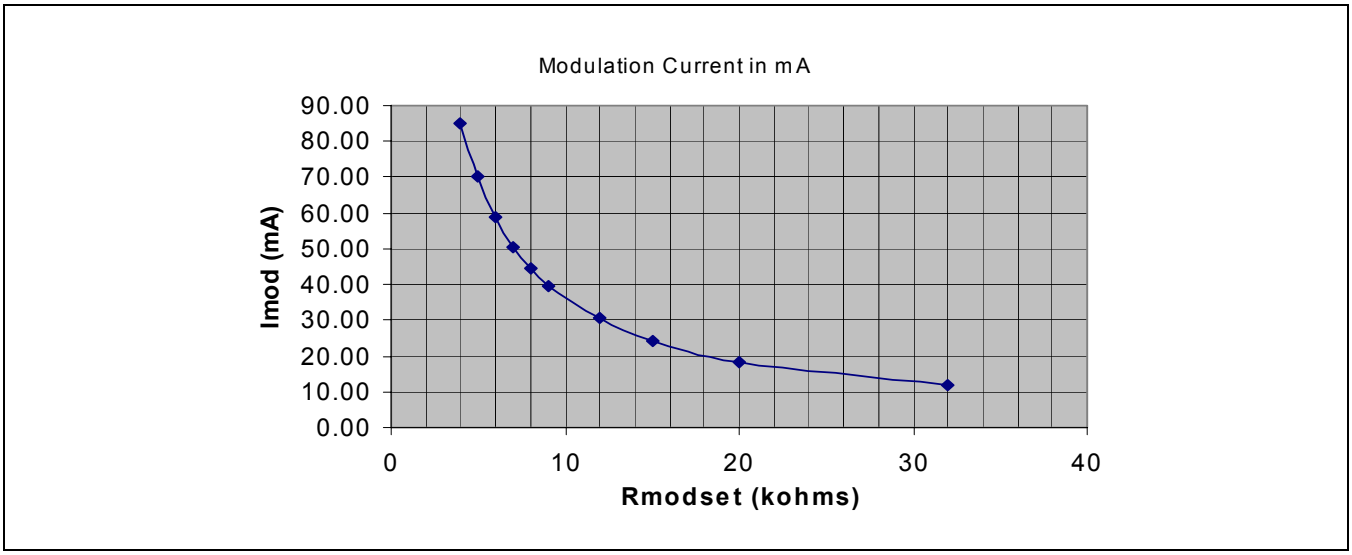
These values will need to be optimized for a specific laser.Any capacitive loading at the cathode of a laser diode will degrade the optical output performance. An inductor is used to isolate the BIAS pin from the laser cathode. See Figure 3-1.

The modulator output stage is designed to drive up to 85mA in either AC-coupled or DC-coupled mode. DC-coupled performance depends on the laser used.

R_{MODSET} determines the modulation current according to the following formula: $I_{MOD} = 350/R_{MODSET}$

Figure 3-2 shows the modulation current for a given R_{MODSET} resistor.

Figure 3-2. Modulation Current vs. R_{MODSET}



3.4 Mean Power Control Loop

To maintain constant average optical power, the M02066 incorporates a control loop to compensate for the changes in laser threshold current over temperature and lifetime. A monitor photodiode mounted in the laser package is used to convert the optical power into a photocurrent. The MPC loop adjusts the laser bias current so that the voltage at PD is matched to an on-chip reference voltage. The external resistor (R_{MPCSET}) sets the optical power.

$R_{MPCSET} = 1.28/I_{PIN}$

I_{PIN} is the mean current from the monitor photodiode at the required mean laser power level (see laser datasheet).The time constant of the loop is determined by C_{MPC}. In some applications the internal capacitance at C_{MPC} may be sufficient and an external C_{MPC} will not be required.

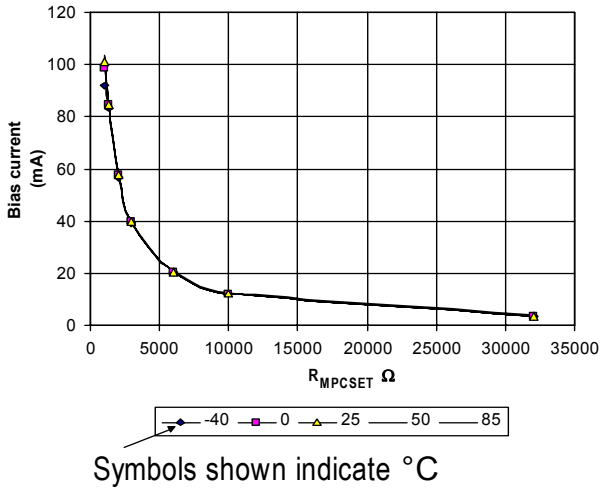
Table 3-1. MPC Loop Bandwidth

C_{MPC}	6 dB cutoff frequency
0	17 MHz
1 nF	100 kHz
10 nF	10 kHz
100 nF	1 kHz

(at 6 dB cut off frequency) vs C_{MPC} (for nominal process)

Figure 3-3 shows the bias current vs R_{MPCSET} over the full operating temperature range.

Figure 3-3. Bias Current vs. R_{MPCSET}

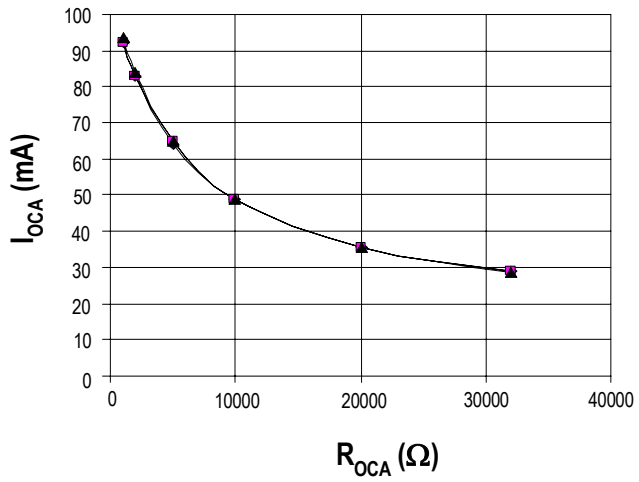


NOTE:
This curve will scale with monitor photodiode current transfer efficiency.

There are two safety features integrated into the MPC loop; an Over-Current Alarm and an MPC loop failure alarm.

The Over-Current Alarm (OCA) circuit limits the maximum bias current generated by the M02060. The bias current limit is set by an external resistor to ground, R_{OCA}. When this limit is exceeded the $\overline{OCA}$ pin is asserted LOW. Figure 3-4 shows the maximum bias current limit vs R_{OCA}.

Figure 3-4. Typical limiting current vs R_{OCA} (at 25 °C)



3.5 Safety Logic

Safety logic is provided in order to limit the maximum bias current. The bias current at which the safety logic trips is set by an external resistor to ground (R_{OCA}) from the OCA_{SET} pin. When the bias current limit is reached alarm flag OCA is asserted LOW. A loop failure alarm is also provided to detect when the bias current can no longer be adjusted to achieve the desired average optical power.

3.6 Data Input Latch

To minimize input data pattern-dependent jitter, a differential clock signal can be connected to the data input latch. If CEN is HIGH, the input data is retimed by the rising edge of CLK+. If CEN is LOW, the input data is directly connected to the output stage. If CEN is left floating it will be pulled HIGH by the internal circuitry. When this latch function is not used, connect CLK+ to V_{CC} and leave CLK- unconnected.

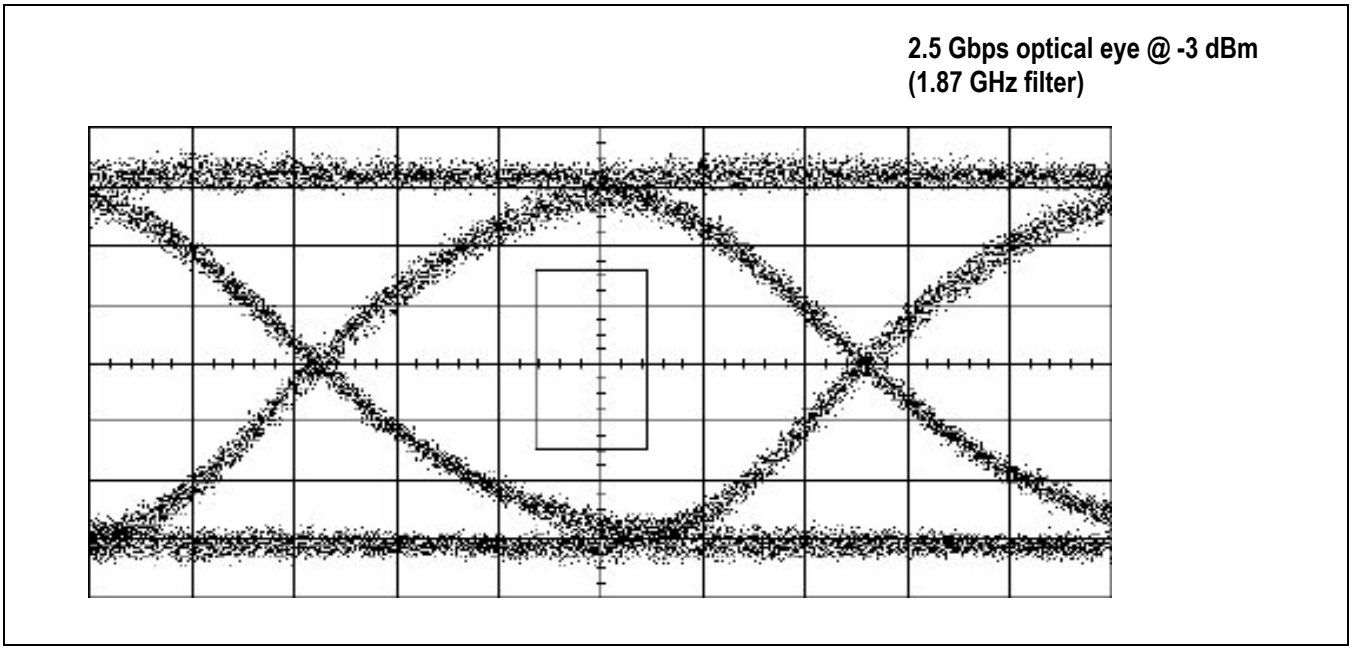
3.7 Enable Control

The M02066 incorporates a dual laser driver enable function. When ENA is LOW or DIS is HIGH, both the bias and modulation currents are off. DIS and ENA are available on the M02066 die only, DIS is available on the BCC package only, ENA is available on the TQPF package.

3.8 Current Monitors

The M02066 features bias and modulation current monitor outputs. The $BIAS_{MON}$ output sinks a current equal to nominally 1/60 of the laser bias current (I_{BIAS}). The MOD_{MON} output sinks a current equal to nominally 1/60 of the laser peak to peak modulation current (I_{MOD}). $BIAS_{MON}$ and MOD_{MON} should be connected through a pull-up resistor to V_{CC}. Choose a pull-up resistor value that ensures a voltage at $BIAS_{MON}$ greater than V_{CC}-1.6V and a voltage at MOD_{MON} greater than V_{CC} - 1.0V. These pins should be tied to V_{CC} if not used.

Figure 3-5. Typical Eye Diagram



3.9 Temperature Compensation

The reduction in slope efficiency of typical laser diodes caused by increased temperature can be compensated by utilising the TC_{START} and TC_{SLOPE} features of the M02066. Under closed loop conditions the average optical power will be maintained by the Mean Power Control loop, compensating for factors such as temperature and age.

However, as the laser slope efficiency reduces with increasing temperature the laser diode will require a greater peak to peak current swing in order to maintain the same peak to peak optical output swing. To this end the M02066 senses temperature and can be programmed to increase the modulation current amplitude accordingly.

Two external resistors are used to program the temperature compensation.

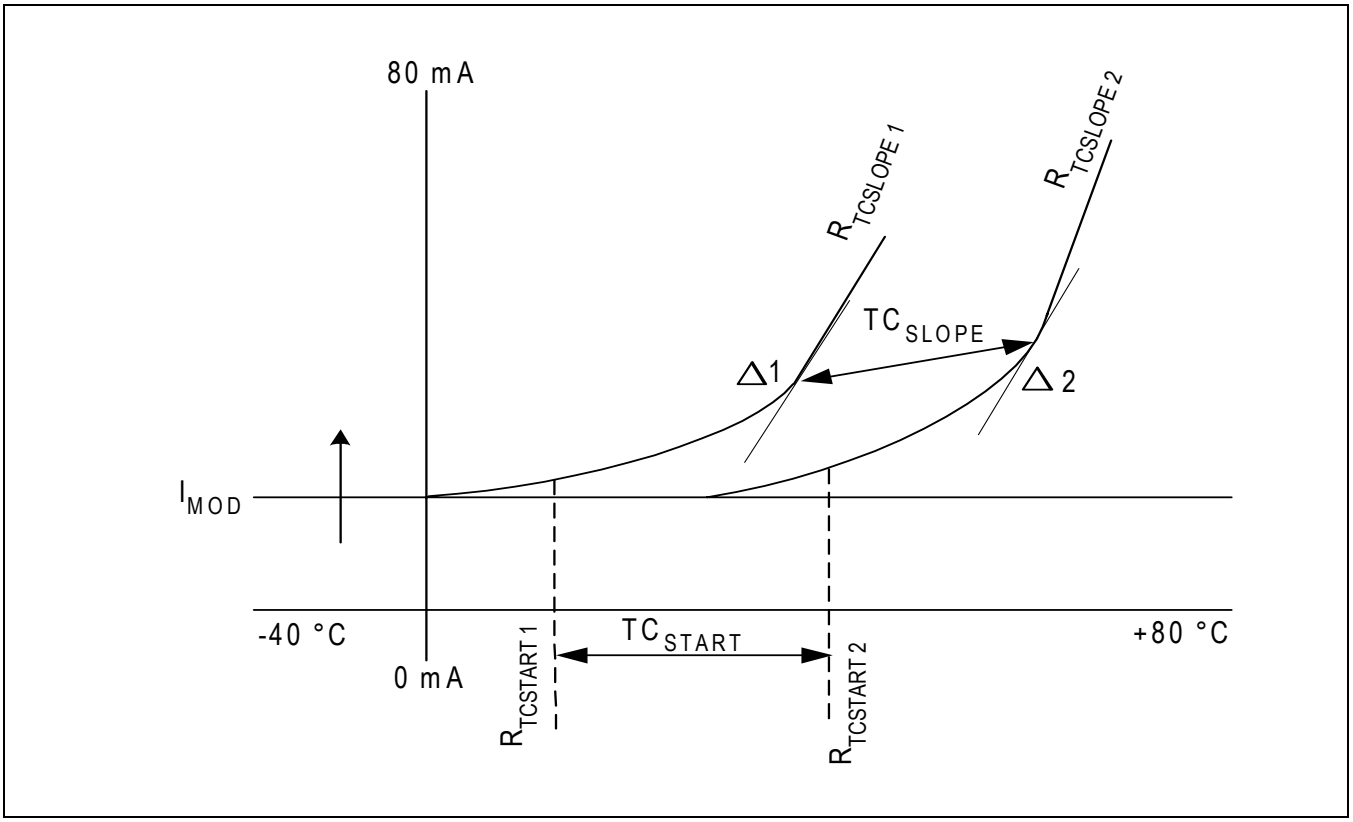
The temperature (TC_{START}) at which the compensation begins to take effect is set by a resistor (RTC_{START}) from the TC_{START} pin to ground. The rate of increase of modulation current with temperature (beyond TC_{START}) is set by a resistor (RTC_{SLOPE}) from the TC_{SLOPE} pin to ground.

As a safety feature, the M02066 limits the increased modulation current to twice the initial (ambient) modulation current.

The effects of the two programming resistors are shown schematically in the Temperature Compensation graph below.
If using the TQFP package; only TC_{SLOPE} is programmable, TC_{START} is connected to 0 V.

For more details on temperature compensation see the appropriate applications note.

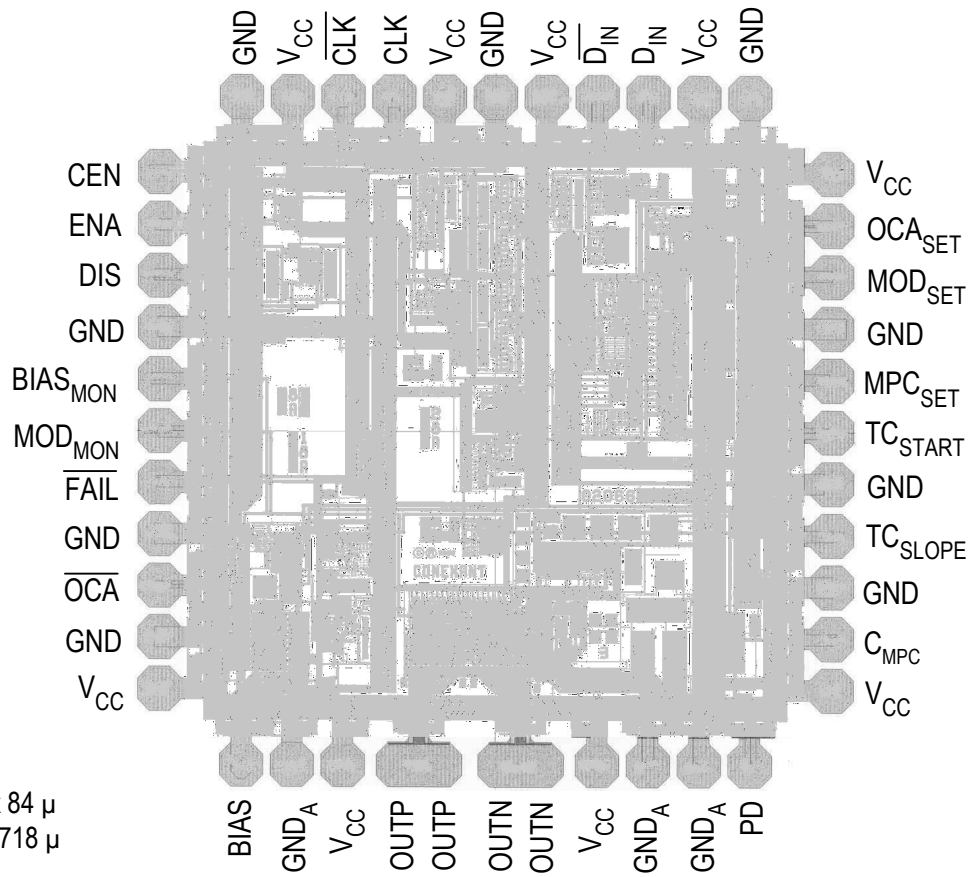
Figure 3-6. Temperature Compensation



4.0 Packaging Specification

4.1 Packaging Specification

Figure 4-1. Bare Die Information



Dimensions:

Pad opening 84 x 84 µ
Die size 1790 x 1718 µ

Table 4-1. Pad Centers

PIN	X	Y	PIN	X	Y	PIN	X	Y	PIN	X	Y
CEN	-727	550	BIAS	-550	-711	V_{CC}	727	-550	GND	550	711
ENA	-727	440	GND_A	-440	-711	C_{MPC}	727	-440	V_{CC}	440	711
DIS	-727	330	V_{CC}	-330	-711	GND	727	-33-	D_{IN}	330	711
GND	-727	220	*OUTP	-210	-711	TC_{SLOPE}	727	-220	D_{IN}	220	711
$BIAS_{MON}$	-727	110	*OUTP	-210	-711	GND	727	-110	V_{CC}	110	711
MOD_{MON}	-727	0	*OUTN	100	-711	TC_{START}	727	0	GND	0	711
FAIL	-727	-110	*OUTN	100	-711	MPC_{SET}	727	110	V_{CC}	-110	711
GND	-727	-220	V_{CC}	220	-711	GND	727	220	CLK	-220	711
OCA	-727	-330	GND_A	330	-711	MOD_{SET}	727	330	CLK	-330	711
GND	-727	-440	GND_A	440	-711	OCA_{SET}	727	440	V_{CC}	-440	711
V_{CC}	-727	-550	PD	550	-711	V_{CC}	727	550	GND	-550	711

NOTE:

* Single pad/double bond

Figure 4-2. TQFP32 Package Information

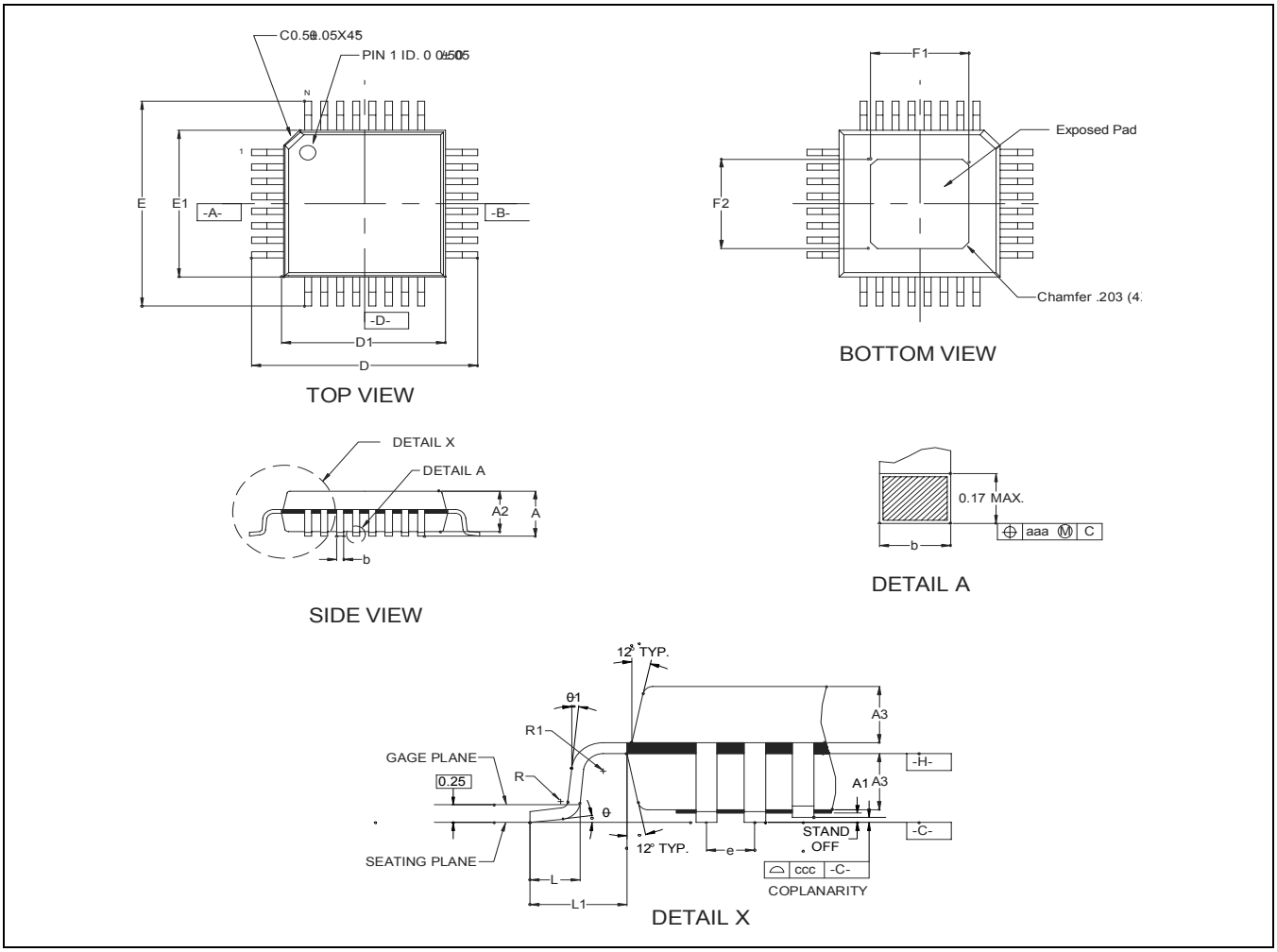


Table 4-2. TQFP32 Package Dimensions

Dim	Tol.	5 x 5 x 1.0 mm	Dim	Tol.	5 x 5 x 1.0 mm
N	Lead count	32	e	Typ.	0.50
A	Max.	1.20	b	±0.05	0.22
A1	±0.05	0.05	0	***	0° - 7°
A2	±0.05	1.00	01	±4°	6°
A3	±0.05	0.4365	R	Max.	0.15
D	±0.15	7.00	R1	Typ.	0.15
D1	±0.05	5.00	aaa	Max.	0.08
E	±0.15	7.00	ccc	Max.	0.08
E1	±0.05	5.00	F1	±0.10	2.67
L	+0.15/-0.15	0.60	F2	±0.10	2.67
L1	Ref.	1.00			

Figure 4-3. BCC+24L Package Information

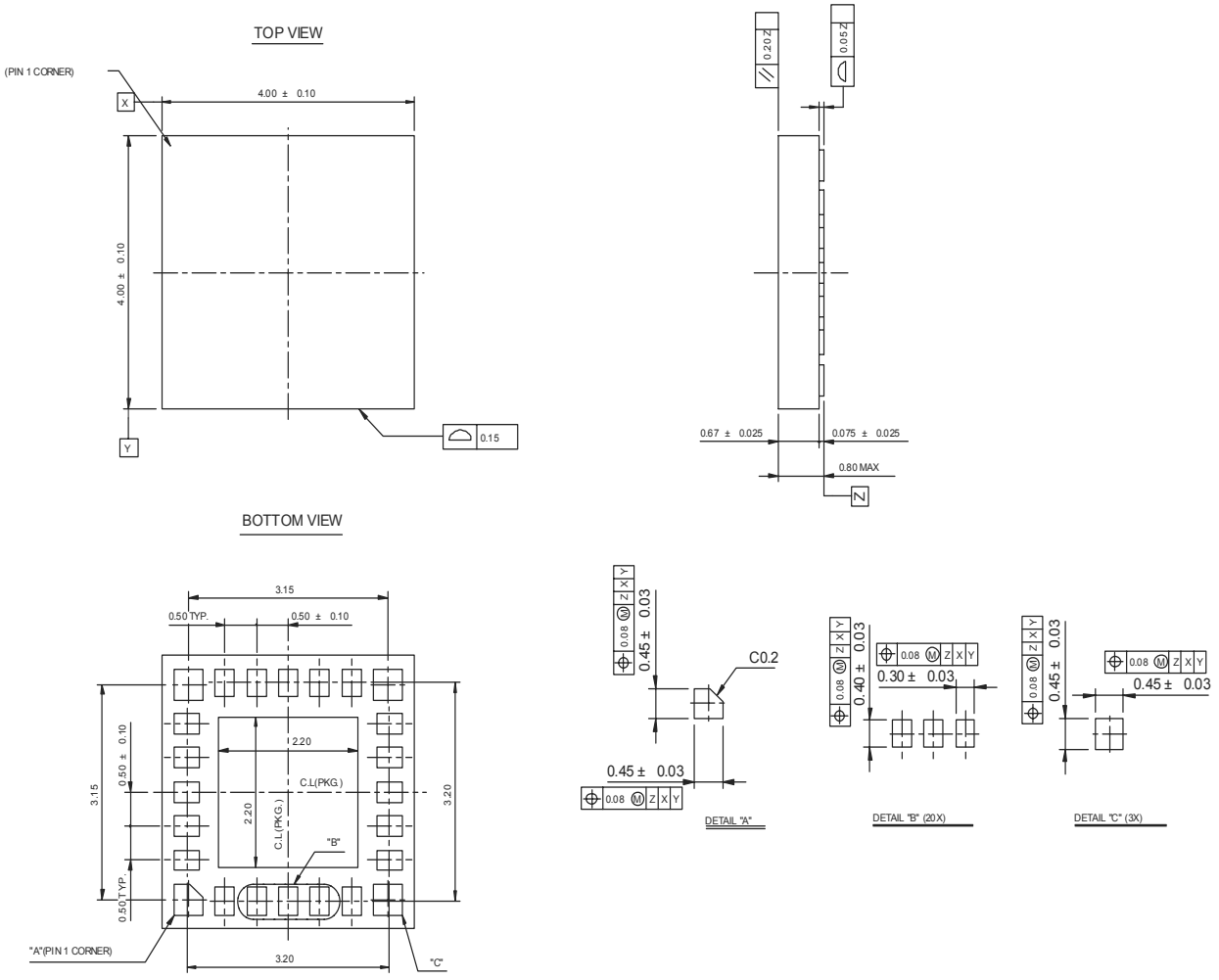


Table 4-3. Features

	DIE	BCC+24	TQFP
ENA	YES	NO	YES
DIS	YES	YES	NO
$BIAS_{MON}$	YES	(1)	YES
MOD_{MON}	YES	(1)	YES
TEMPCOMP	YES	YES	(2)
SIZE (mm)	1.79 x 1.72	4 x 4	5 x 5

NOTES:

1. $BIAS_{MON}$ and MOD_{MON} current sinks are common on pin 4.
2. $R_{TCSTART}$ = 0 Ω (internally bonded) $R_{TCSLOPE}$ can be used on pin 28.

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