STB4NK60Z, STB4NK60Z-1, STD4NK60Z, STD4NK60Z-1

N-channel 600 V, 1.7 Ω typ., 4 A Zener-protected SuperMESH™ Power MOSFETs in D²PAK, I²PAK, DPAK and IPAK packages

Datasheet - production data

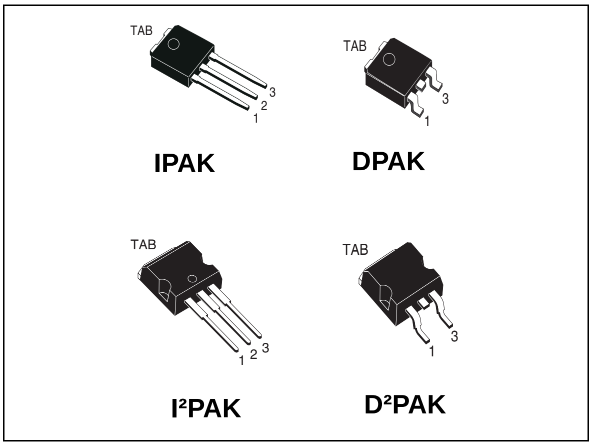
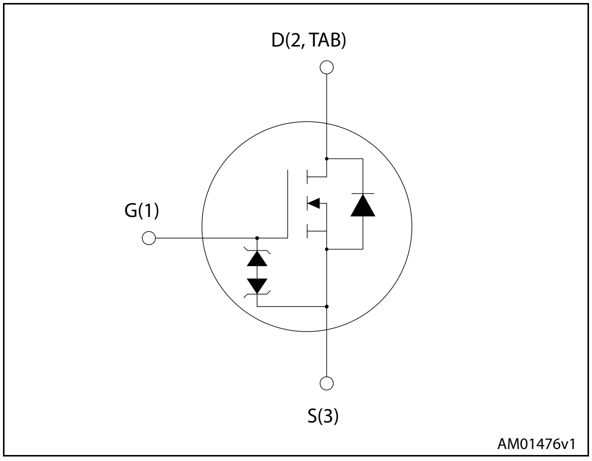


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	P_{TOT}	I_D
STB4NK60ZT4	600 V	2 Ω	70 W	4 A
STB4NK60Z-1				
STD4NK60ZT4				
STD4NK60Z-1				

- 100% avalanche tested
- Very low intrinsic capacitances
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB4NK60ZT4	B4NK60Z	D^2PAK	Tape and reel
STB4NK60Z-1		I^2PAK	Tube
STD4NK60ZT4	D4NK60Z	DPAK	Tape and reel
STD4NK60Z-1		IPAK	Tube

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	4	A
I_D	Drain current (continuous) at T_C = 100 °C	2.5	A
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
	Derating factor	0.56	W/°C
ESD	Gate-source human body model (C=100 pF, R=1.5 kΩ)	3	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 4$ A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK, I^2PAK	DPAK, IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.79		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	100	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AR}, V_{DD}= 50 V)	120	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D =1 mA	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C = 125 °C			1 50	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 μA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2 A		1.7	2	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2 A	-	3		S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	510		pF
C_{oss}	Output capacitance		-	67		pF
C_{rss}	Reverse transfer capacitance		-	13		pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS} =0, V_{DS} = 0 to 480 V	-	38.5		pF
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	12		ns
t_r	Rise time		-	9.5		ns
$t_{d(off)}$	Turn-off delay time		-	29		ns
t_f	Fall time		-	16.5		ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 480 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	12		ns
t_r	Fall time		-	12		ns
t_c	Cross-over time		-	19.5		ns
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 4 A, V_{GS} = 10 V (see *Figure 16*)	-	18.8	26	nC
Q_{gs}	Gate-source charge		-	3.8		nC
Q_{gd}	Gate-drain charge		-	9.8		nC

1. Pulsed: pulse duration=300μs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
I_{SDM}(1)	Source-drain current (pulsed)		-		16	A
V_{SD}(2)	Forward on voltage	I_{SD} = 4 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4 A, di/dt = 100 A/μs V_{DD} = 24 V, Tj = 150 °C (see *Figure 17*)	-	400		ns
Q_{rr}	Reverse recovery charge		-	1700		nC
I_{RRM}	Reverse recovery current		-	8.5		A

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device’s ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

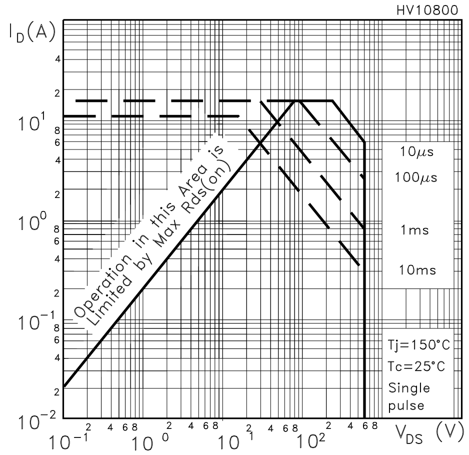


Figure 3. Thermal impedance

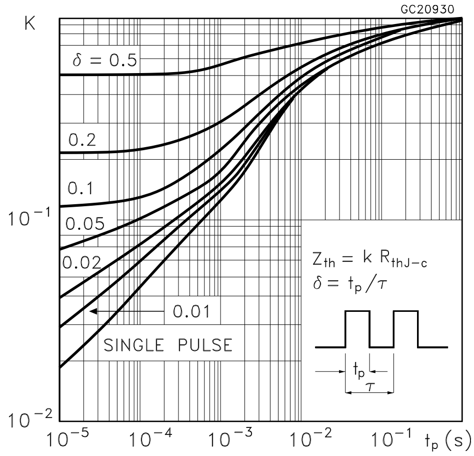


Figure 4. Output characteristics

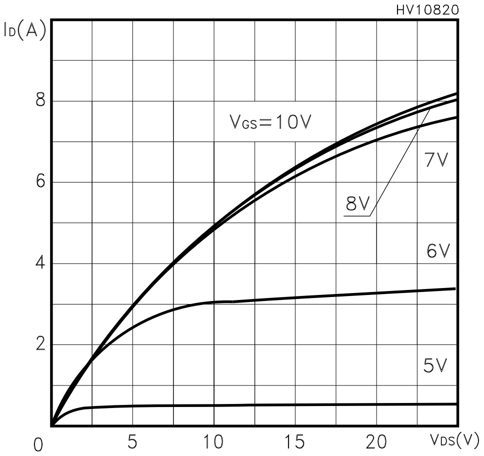


Figure 5. Transfer characteristics

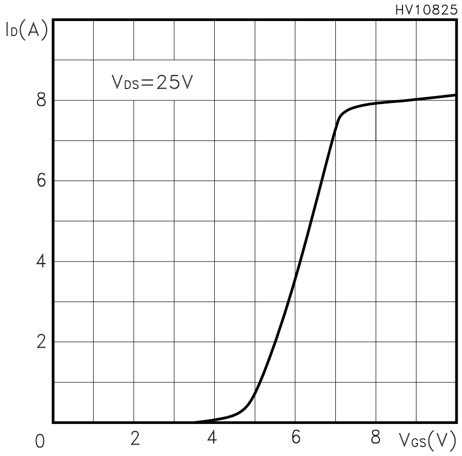


Figure 6. Transconductance

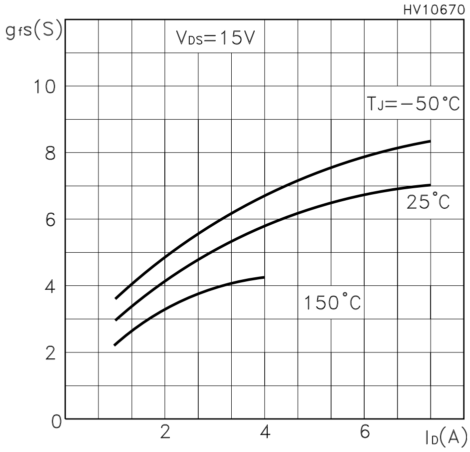


Figure 7. Static drain-source on-resistance

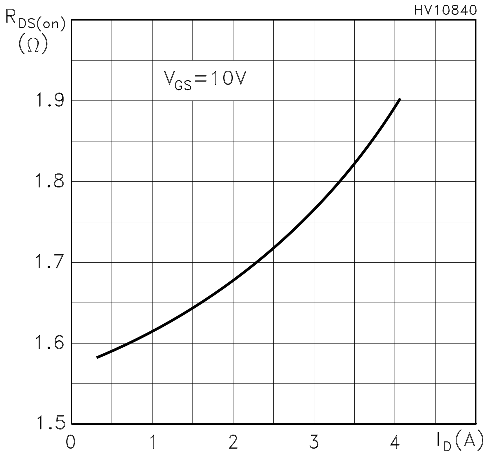


Figure 8. Gate charge vs gate-source voltage

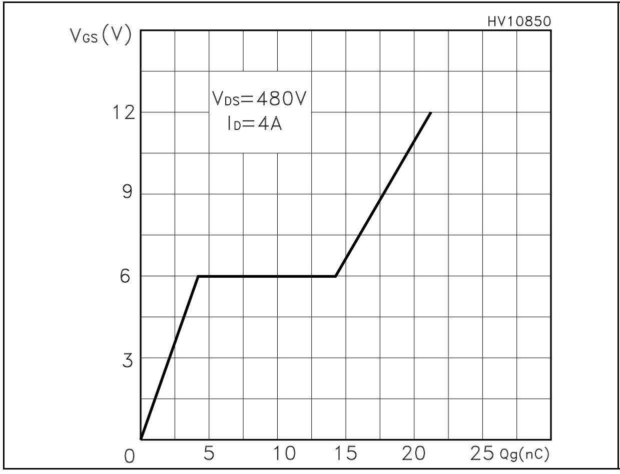


Figure 9. Capacitance variations

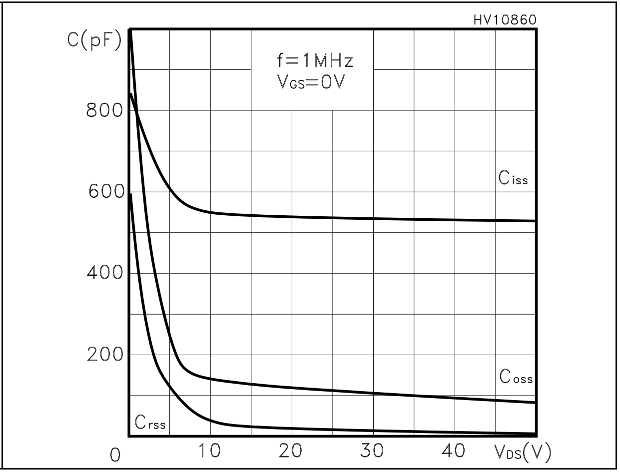


Figure 10. Normalized gate threshold voltage vs temperature

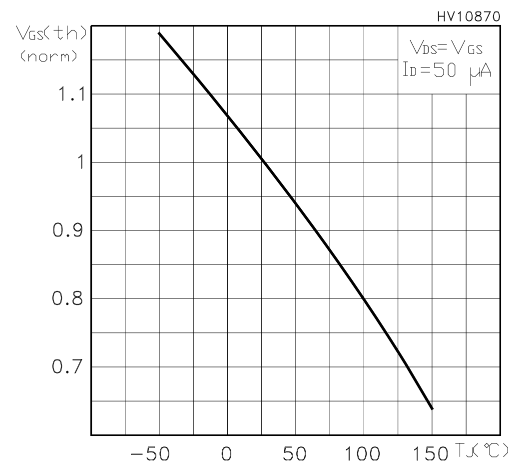


Figure 11. Normalized $R_{DS(on)}$ vs temperature

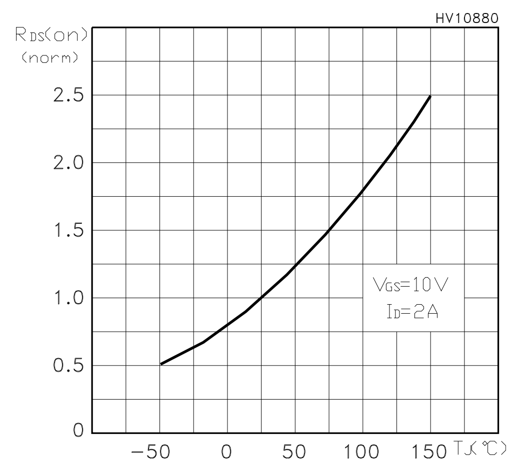


Figure 12. Source-drain diode forward characteristic

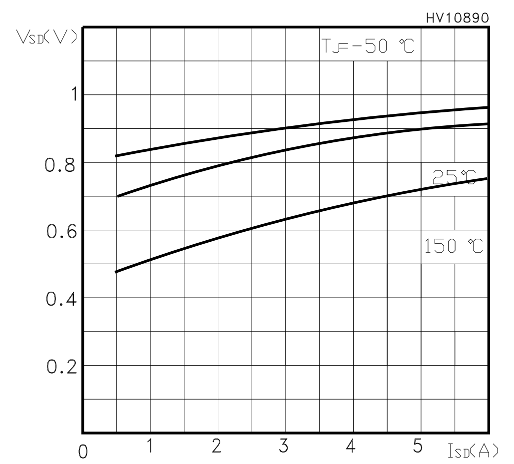


Figure 13. Normalized V_{DS} vs temperature

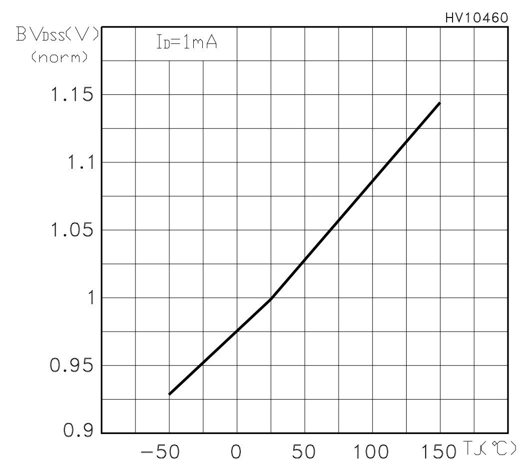
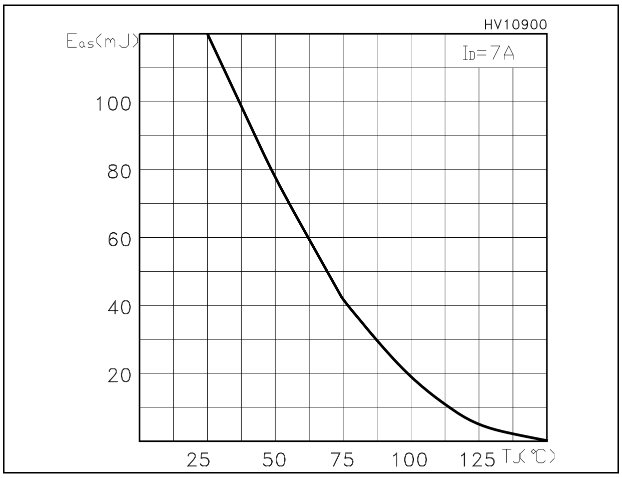


Figure 14. Avalanche energy vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load

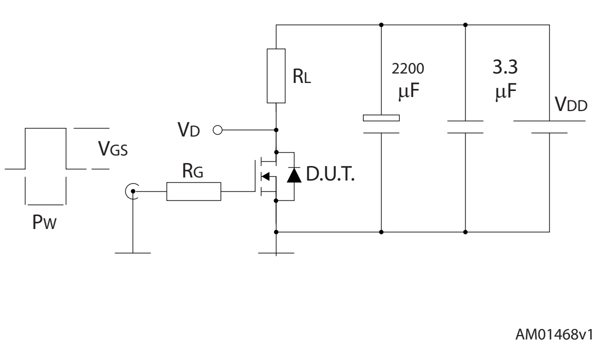


Figure 16. Gate charge test circuit

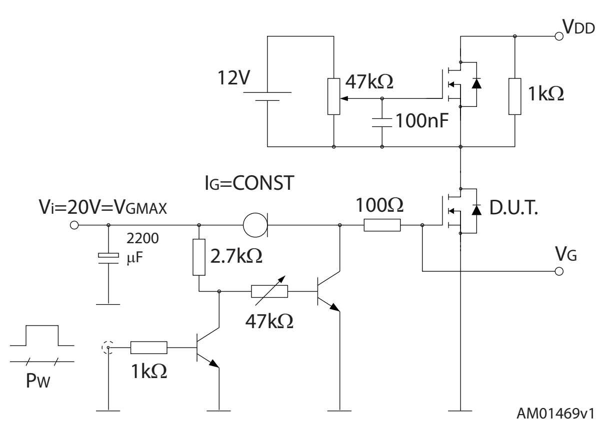


Figure 17. Test circuit for inductive load switching and diode recovery times

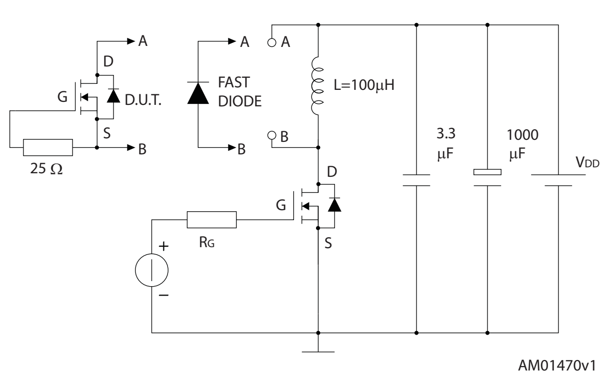


Figure 18. Unclamped inductive load test circuit

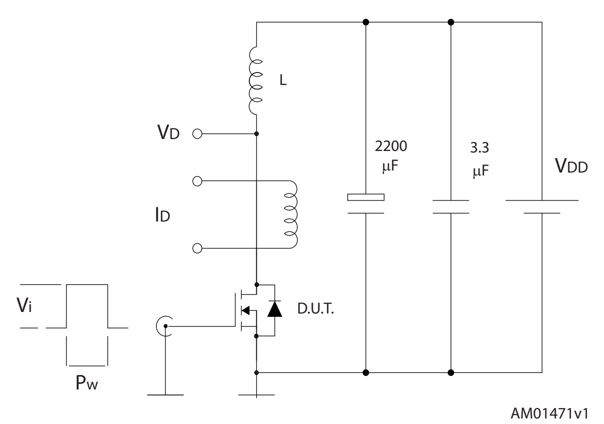


Figure 19. Unclamped inductive waveform

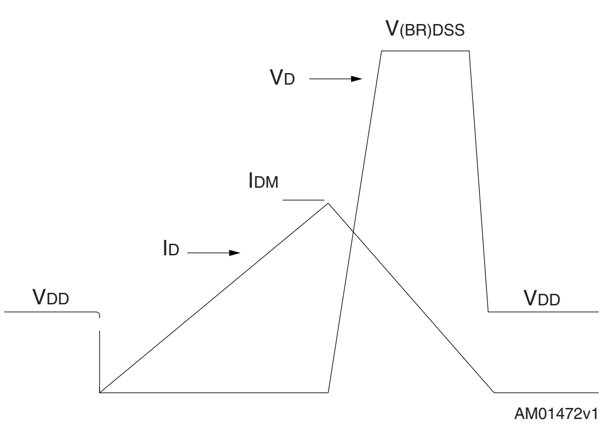
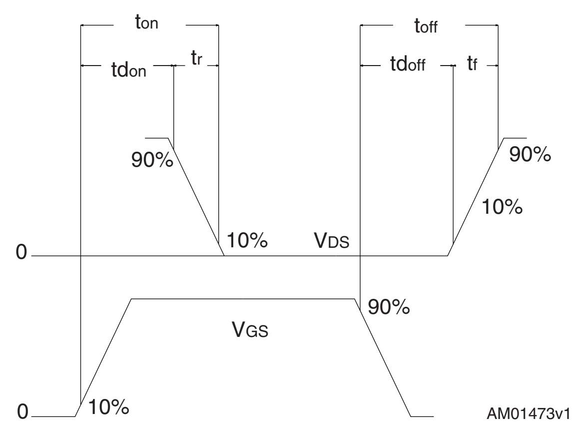


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

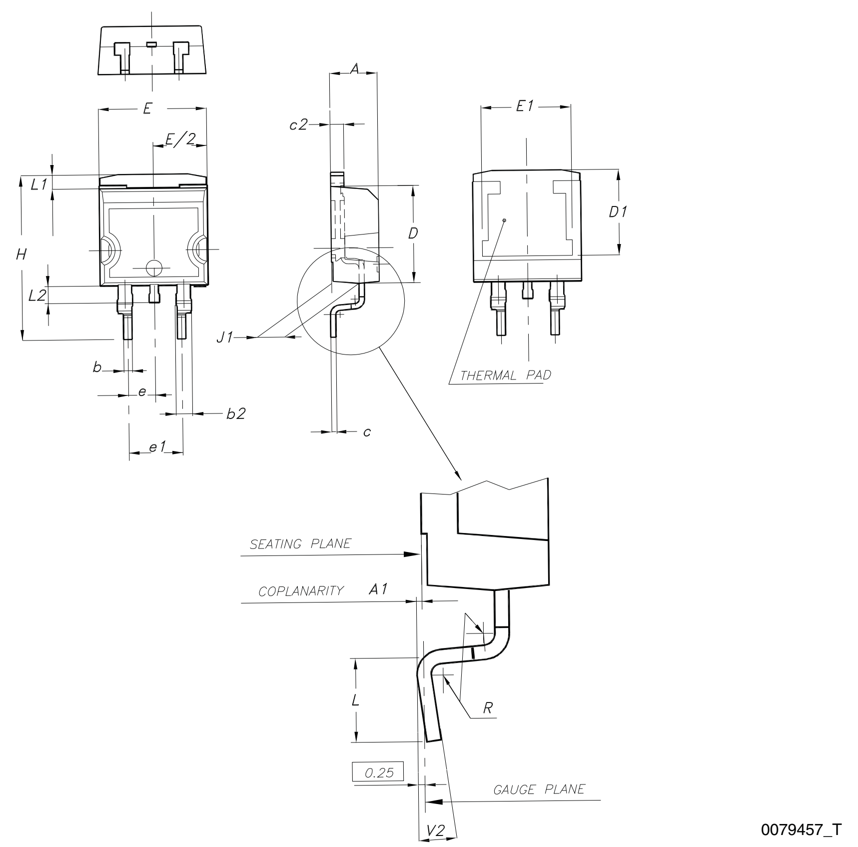


Figure 21. D²PAK (TO-263) drawing

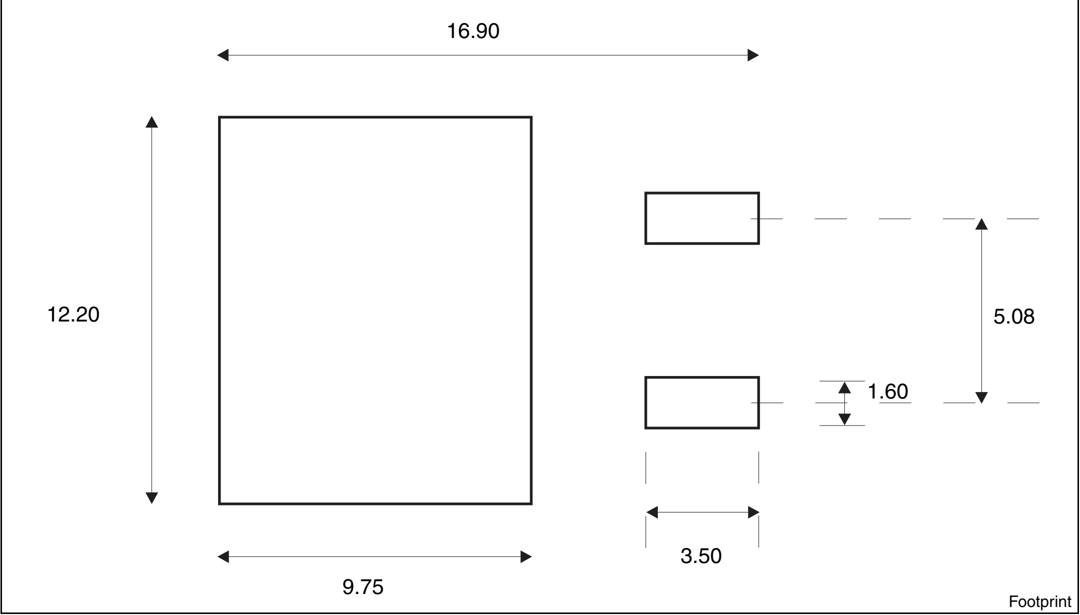


Figure 22. D²PAK footprint[a]

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[a] All dimension are in millimeters

Table 10. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 23. I²PAK (TO-262) drawing

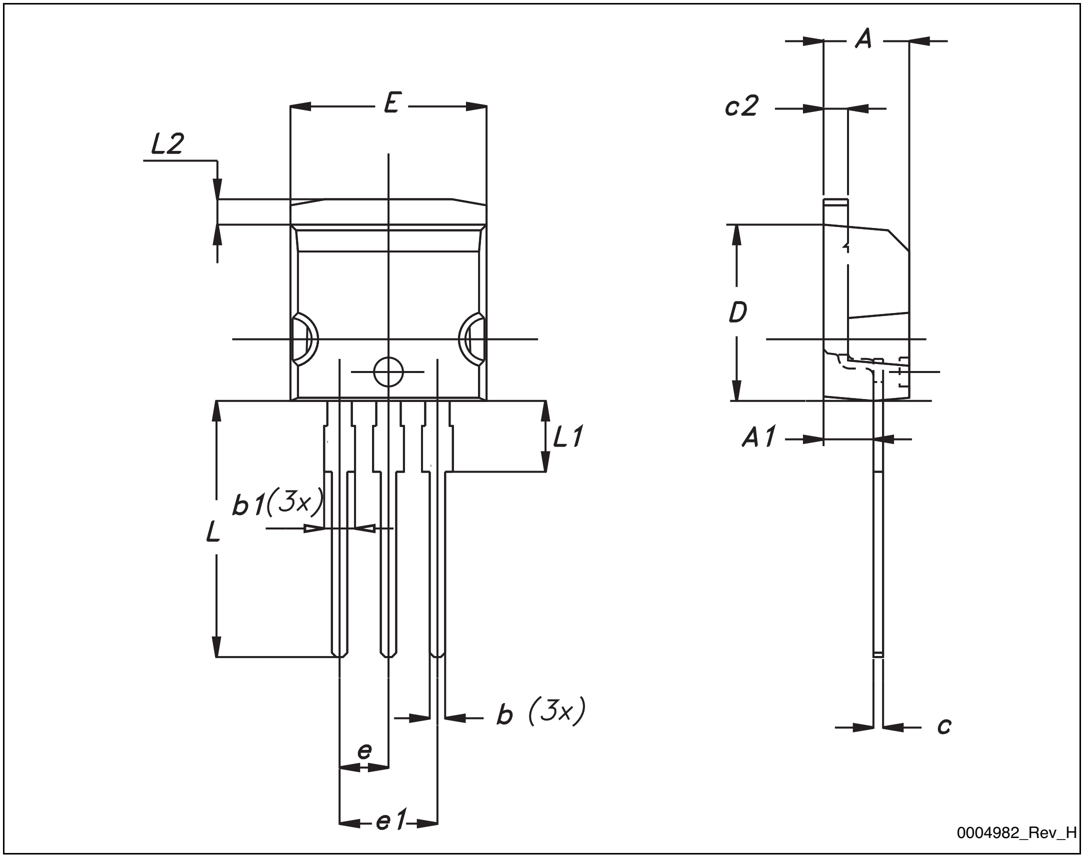


Table 11. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) type A drawing

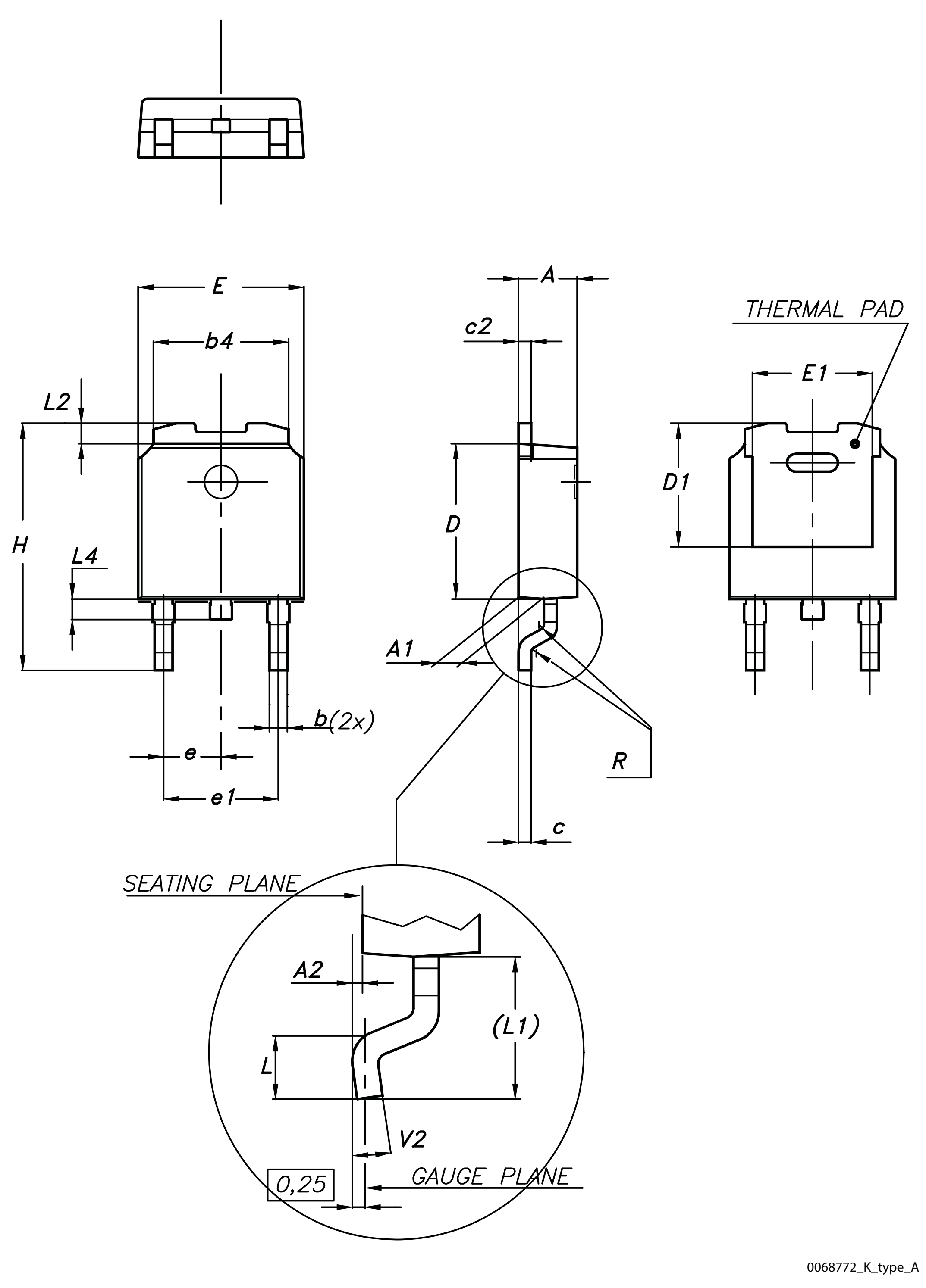


Table 12. DPAK (TO-252) type E mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 25. DPAK (TO-252) type E drawing

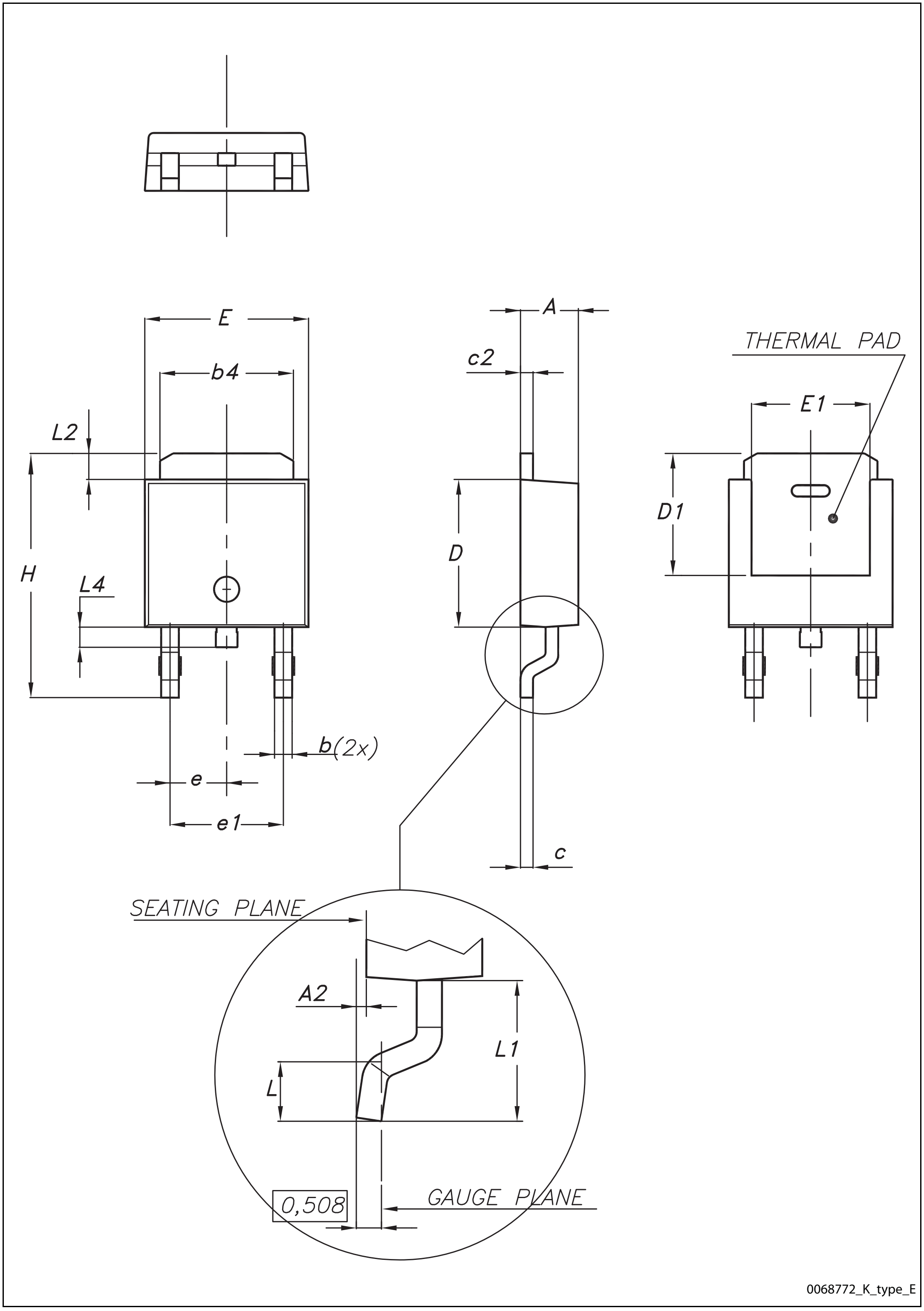
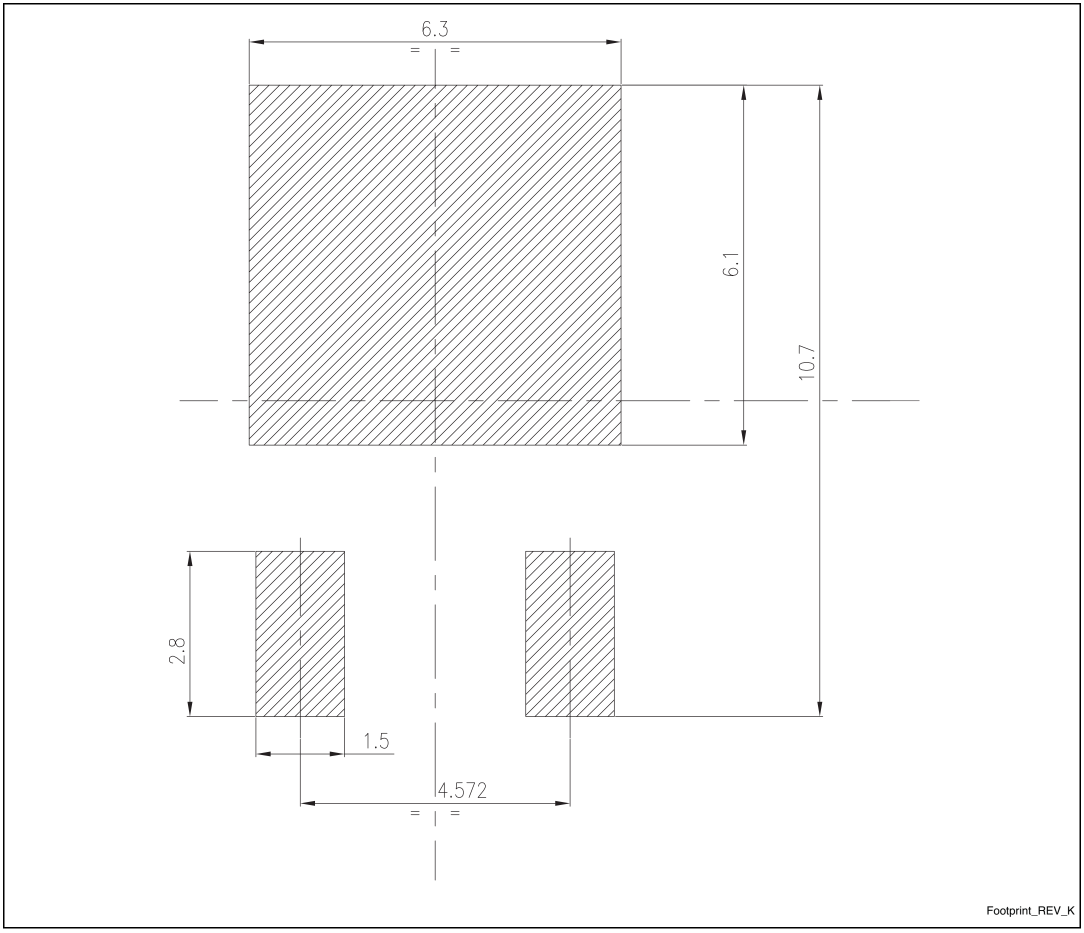


Figure 26. DPAK footprint [b]



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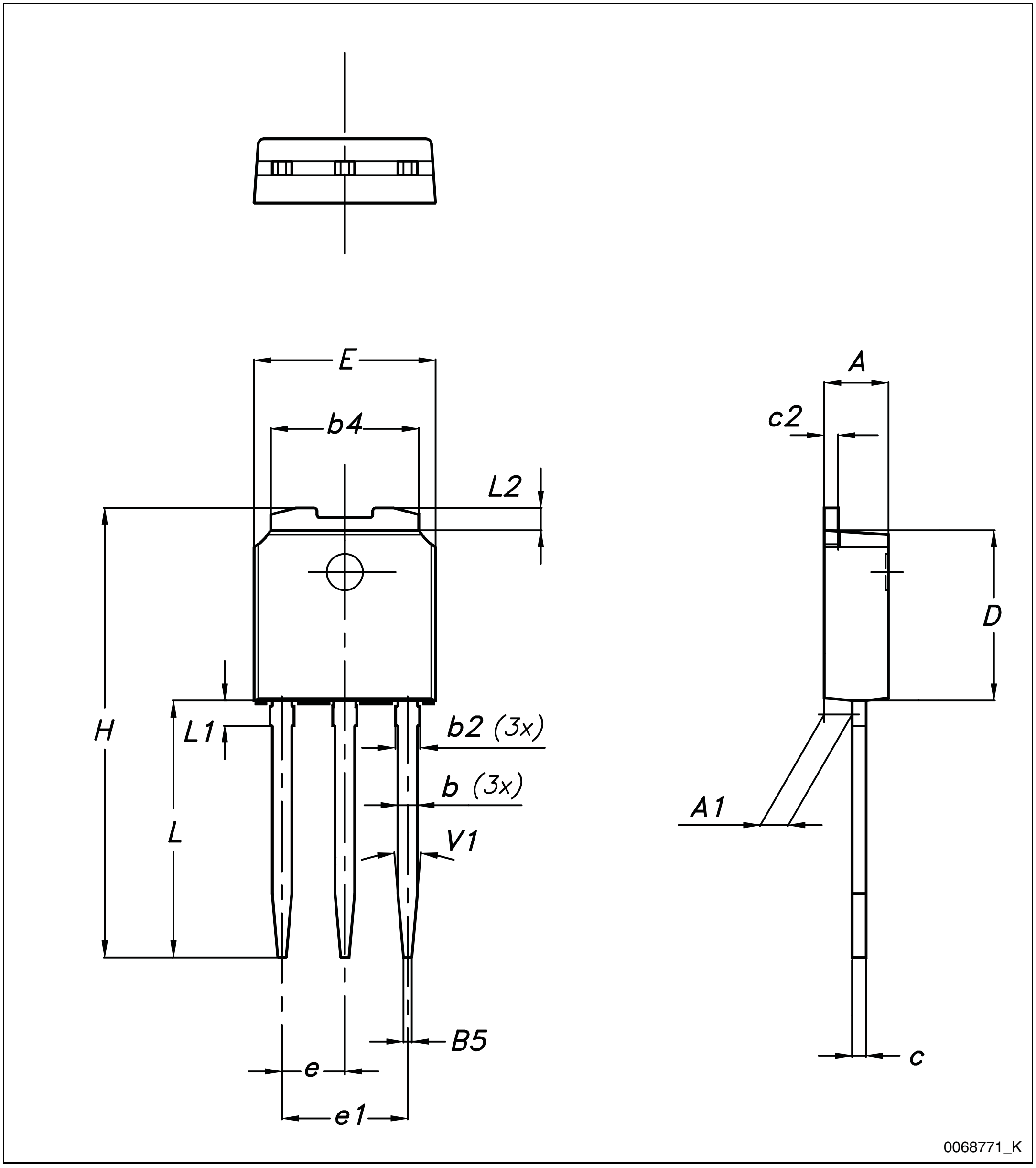
[b] All dimensions are in millimeters

Table 13. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 27. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 14. D^2PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 15. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 28. Tape

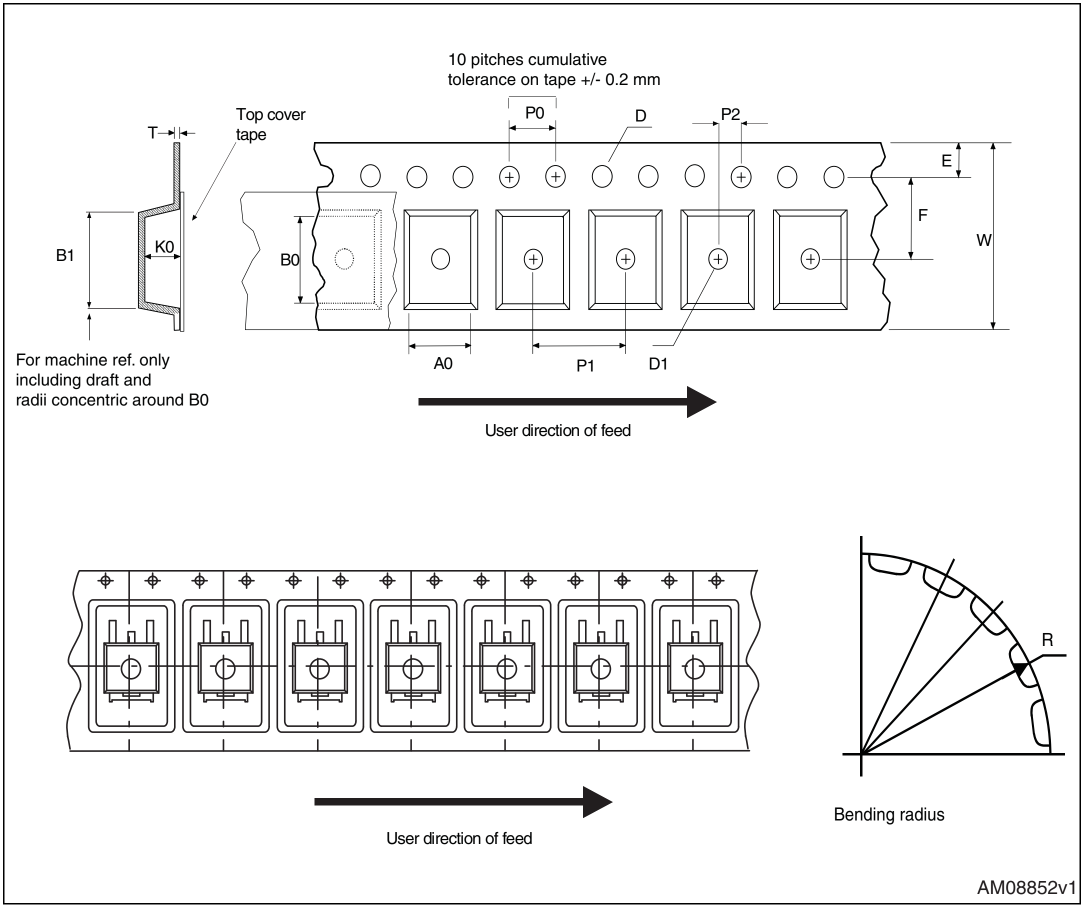
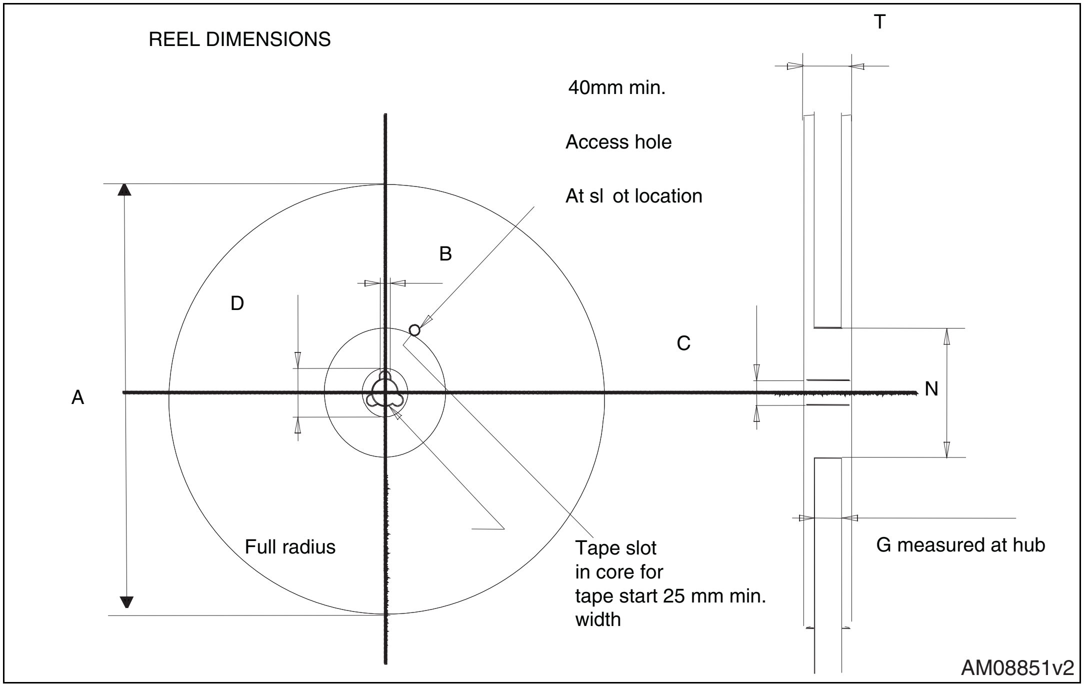


Figure 29. Reel



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
25-Oct-2006	4	Document reformatted no content change.
04-Mar-2008	5	Modified TO-220 and TO-220FP mechanical data.
16-Apr-2008	6	Minor text changes to improve readability.
11-Jul-2011	7	Updated package mechanical data *Section 4* and packaging mechanical data *Section 4*.
18-Jul-2013	8	– Minor text changes – The part numbers STP4NK60Z and STP4NK60ZFP have been moved to a separate datasheet – Updated: *Section 4: Package mechanical data* and *Section 4: Package mechanical data*

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