

# Dual-core, highly secure, energy-efficient MCU

# K32 L3 MCU Family

Building on the success and wide adoption of the Kinetis MCU portfolio, the K32 L3 MCU family is designed to deliver a power-optimized implementation along with advanced security capabilities and protection from physical tamper events.

### TARGET APPLICATIONS

- ▶ Building automation
  - Security and access control
  - Building control and monitoring
  - Building HVAC control
  - Secure applications
- ▶ Industrial
  - Factory automation
  - Robotics
- ▶ Smart home
  - Door locks
  - Smart thermostats
  - Lighting control
  - Security systems

### **OVERVIEW**

The K32 L3 MCU family delivers significant improvements in power optimization and security advancements to address a wide range of industrial and IoT applications. The K32 L3 family provides new enhancements such as low-leakage, power-optimized peripherals, a DC-DC converter, and security features like authenticated boot, secure update and tamper detection pins.

The K32 L3 family includes a high-performance Arm® Cortex®-M4 processor and a low-power Cortex-M0+ processor, ideal for applications that require a host MCU

and a low-power MCU. With up to 1.25 MB flash and up to 384 kB SRAM, the K32 L3 family offers ample memory resources to address different applications tasks in a small form factor, low-power, and highly secure design.

The introduction of the K32 L3 family is the start of a long line of MCUs which will further advance our security and power optimization to lead the market in next-generation, power-conscious and low-leakage applications.

Take advantage of the robust enablement to reduce development effort and speed time-to-market with NXP's comprehensive offering of development tools and MCUXpresso software providing an open-source software development kit (SDK), an easy-to-use integrated development environment (IDE) and a comprehensive suite of system configuration tools.

## **ENABLEMENT**

- FRDM-K32L3A6 Freedom development board
- Support for NXP's MCUXpresso and IAR Embedded Workbench® IDEs
- ▶ Full integration with NXP's MCUXpresso SDK
- ▶ Support for multiple RTOSes including FreeRTOS™



## **K32 L3 MCU FAMILY BLOCK DIAGRAM**

| Core Platform  |                       | Timers                           |                       |  |
|--|-----------------------|----------------------------------|-----------------------|--|
| Arm <sup>®</sup> Cortex <sup>®</sup> -M4<br>Up to 72 MHz |                       | LPIT 2x<br>(4 Channel)           | LPTMR 3x<br>(32-bit)  |  |
| DSP, sFPU, NVIC, SysTick  Arm Cortex-M0+                 |                       | TPM 2x<br>(6 Channel)            | TPM 2x<br>(2 Channel) |  |
| Up to 72 MHz   |                       | Time Stamp Timer                 | Real-Time Clock       |  |
| Division, Square F                                       | Root, NVIC, Systick   |                                  | •                     |  |
|  |                       | Communication and HMI Interfaces |                       |  |
| System   | Control               | EMVSIM                           | External Bus          |  |
| DMA  | Trigger Multiplexer   | FlexIO                           | GPIO                  |  |
| System CLK Generator                                     | Peripheral CLK CTRL   | LP I <sup>2</sup> C 4x           | SAI                   |  |
| System PWR Management                                    | Low-Leakage Wake-Up   | SDHC                             | LP SPI 4x             |  |
| External Watchdog  | Watchdog              | LP UART 4x                       | USB                   |  |
| Memory   |                       | Security                         |                       |  |
| FLASH<br>Up to 1.25 MB                                   |                       | CAU                              | Tamper                |  |
| RAM<br>Up to 384 kB                                      |                       | CRC                              | Resource Domain CTRL  |  |
| Boot ROM<br>48 kB  |                       | Random NUM Generator             |                       |  |
| Clocks   |                       | Analog                           |                       |  |
| LP FLL SIRC<br>48/72 MHz 2/8 MHz                         |                       |                                  |                       |  |
| FIRC<br>48/52/56/60 MHz                                  | RTC OSC<br>32.768 kHz | Dual Output DC/DC                | LP CMP 2x             |  |
|  |                       | Battery Monitor                  | Temperature Sensor    |  |

### **K32 L3 MCU FAMILY KEY FEATURES AND BENEFITS**

| Features                       | Benefits   |
|--------------------------------|--|
| Dual-Core Architecture         | The dual-core feature (72 MHz Arm® Cortex®-M4 core and Cortex M0+ core) of this family makes it ideal for applications that require a high-performance host process to run the application and a low-power processor for low-throughput operations   |
| Large On-Chip Memory           | Ample memory resources (with up to 1.25 MB flash, up to 384 kB SRAM and 48 kB ROM (Bootloader)) to fit different custom application code and data, reducing complex two-chip solutions to a single device  |
| High Security                  | <ul> <li>Resource Domain Controller for access control, system memory protection and peripheral isolation</li> <li>Cryptographic subsystem that includes a dedicated core, dedicated instruction memory (IRAM and IROM) and dedicated data RAM for autonomous implementation of encryption, signing, and hashing algorithms including AES, DES, SHA, RSA and ECC</li> <li>Secure key management for storing and protecting sensitive security keys</li> <li>Wiping of the crypto subsystem memory, including security keys, upon sensing a security breach or physical tamper event</li> </ul> |
| Secure Boot                    | Built-in secure boot to assure only authorized and authenticated code runs in the device   |
| DC-DC Converter                | Reduces the effective current consumption over standard bypass mode  |
| Analog                         | High-performance on-chip analog (ADC, DAC, CMP) for sensor aggregation and other sophisticated applications  |
| Small, High Pin-Count Packages | Large I/O capability in different packages including BGA, LQFP and QFN   |
| Comprehensive Enablement       | Complete development hardware, software stacks, drivers and RTOS for easy design and fast time-to-market   |

# **ORDERABLE PART NUMBER**

| Produc        | t            | Mer     | nory   | С         | ore        | Package                                    |
|---------------|--------------|---------|--------|-----------|------------|--|
| Part Number   | Availability | Flash   | SRAM   | Cortex-M4 | Cortex-M0+ | Package                                    |
| K32L3A60VPJ1A | Q3 2019      | 1.25 MB | 384 kB | J         | √          | 176 VFBGA<br>9 x 9 x 0.86mm<br>0.5mm pitch |