

SOP-8

Pin Definition:

- | | |
|-------------|------------|
| 1. Source 1 | 8. Drain 1 |
| 2. Gate 1 | 7. Drain 1 |
| 3. Source 2 | 6. Drain 2 |
| 4. Gate 2 | 5. Drain 2 |

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
450	4.25 @ $V_{GS}=10V$	0.25

General Description

The TSM1N45 is N-Channel enhancement mode power field effect transistors are produced using planar DMOS technology process.

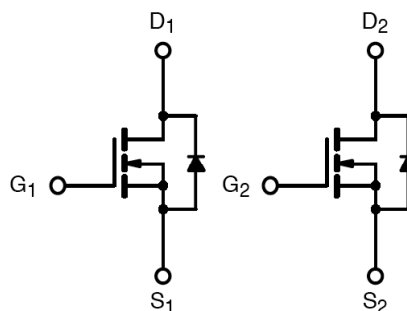
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand higher energy pulse in the avalanche and commutation mode. These devices are well suited for electronic ballasts base and half bridge configuration.

Features

- Low gate charge @ typical 6.5nC
- Low Crss @ typical 6.5pF
- Avalanche energy specified
- Improved dv/dt capability
- Gate-Source Voltage $\pm 50V$ guaranteed

Ordering Information

Part No.	Package	Packing
TSM1N45DCS RL	SOP-8	2.5Kpcs / 13" Reel

Block Diagram


Dual N-Channel MOSFET

Absolute Maximum Rating ($T_a = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	450	V
Gate-Source Voltage	V_{GS}	± 50	V
Continuous Drain Current	I_D	0.5	A
Pulsed Drain Current (Note 1)	I_{DM}	4	A
Single Pulse Drain to Source Avalanche Energy (Note 2)	E_{AS}	108	mJ
Avalanche Current (Note 1)	I_{AR}	0.5	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	0.25	mJ
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5.5	V/ns
Maximum Power Dissipation @ $T_a = 25^\circ C$	P_D	0.9	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Ambient	$R_{\theta JA}$	80	$^\circ C/W$

Notes: Surface mounted on FR4 board $t \leq 10sec$

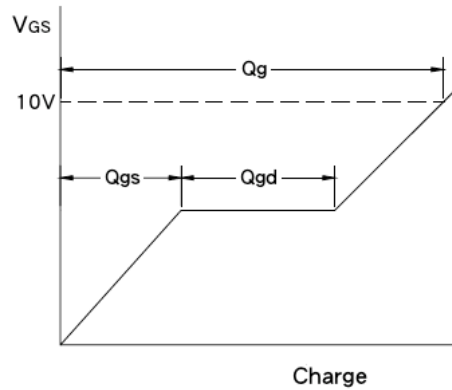
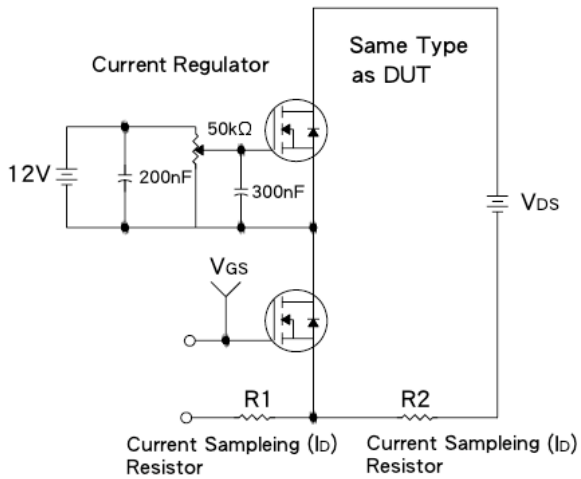
Electrical Specifications (Ta=25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	450	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 0.25A$	$R_{DS(ON)}$	--	3.4	4.25	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.3	3.0	3.7	V
	$V_{DS} = V_{GS}, I_D = 250mA$		3.0	4.2	4.9	
Zero Gate Voltage Drain Current	$V_{DS} = 450V, V_{GS} = 0V$	I_{DSS}	--	--	10	μA
Gate Body Leakage	$V_{GS} = \pm 50V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Forward Transconductance	$V_{DS} = 50V, I_D = 0.25A$	g_{fs}	--	0.7	--	S
Diode Forward Voltage	$I_S = 1A, V_{GS} = 0V$	V_{SD}	--	--	1.5	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 360V, I_D = 0.5A,$ $V_{GS} = 10V$ (Note 4,5)	Q_g	--	6.5	--	nC
Gate-Source Charge		Q_{gs}	--	0.9	--	
Gate-Drain Charge		Q_{gd}	--	3.2	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	185	--	pF
Output Capacitance		C_{oss}	--	29	--	
Reverse Transfer Capacitance		C_{rss}	--	6.5	--	
Switching ^c						
Turn-On Delay Time	$V_{GS} = 25V, I_D = 0.5A,$ $V_{DS} = 225V, R_G = 25\Omega$ (Note 4,5)	$t_{d(on)}$	--	7.5	--	nS
Turn-On Rise Time		t_r	--	21	--	
Turn-Off Delay Time		$t_{d(off)}$	--	23	--	
Turn-Off Fall Time		t_f	--	36	--	
Drain-Source Diode Characteristics and Maximum Ratings						
Maximum Continuous Drain-Source Diode Forward Current		I_S	--	--	0.5	A
Maximum Pulsed Drain-Source Diode Forward Current		I_{SM}	--	--	4.0	A
Drain-Source Diode Forward Voltage	$V_{GS} = 25V, I_S = 0.5A$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$V_{GS} = 25V, I_S = 0.5A,$ $di_F/dt = 100A/\mu S$ (Note 4)	t_{rr}	--	102	--	nS
Reverse Recovery Charge		Q_{rr}	--	0.26	--	μC

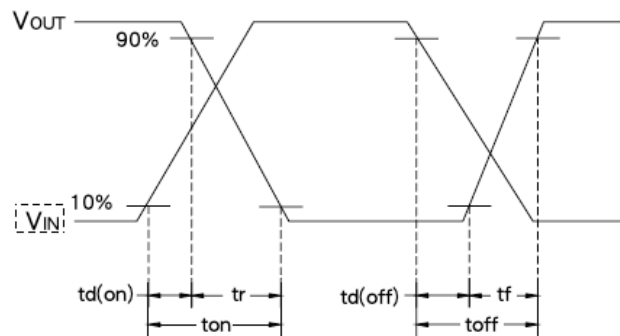
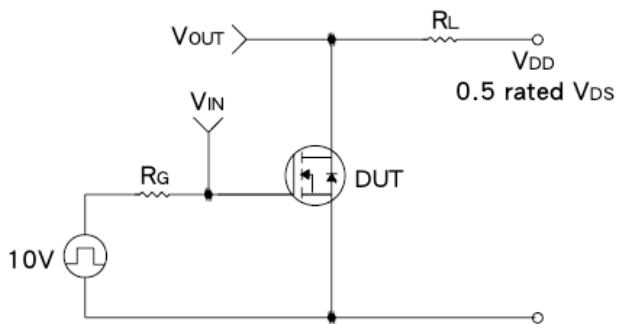
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=75mH, I_{AS}=1.6A, V_{DD}=50V, R_G=25 Ω , Starting T_J=25°C
3. I_{SD} ≤ 0.5A, di/dt ≤ 300A/ μ S, V_{DD} ≤ BV_{DSS}, Starting T_J=25°C
4. Pulse test: pulse width ≤ 300 μ S, duty cycle ≤ 2%
5. Essentially independent of operating temperature
6. a) Reference point of the is the drain R θ_{JL} lead
b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment (R θ_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance. R θ_{CA} is determined by the user's board design)

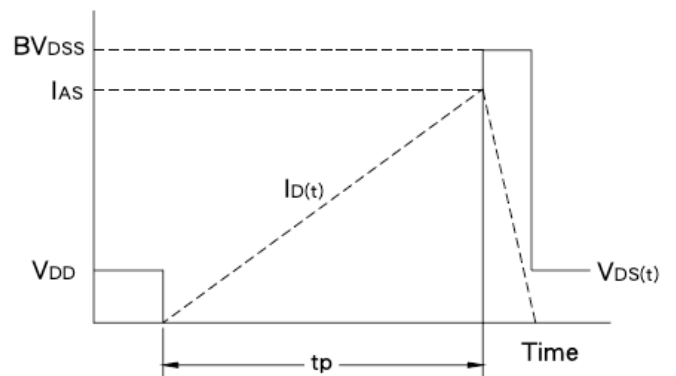
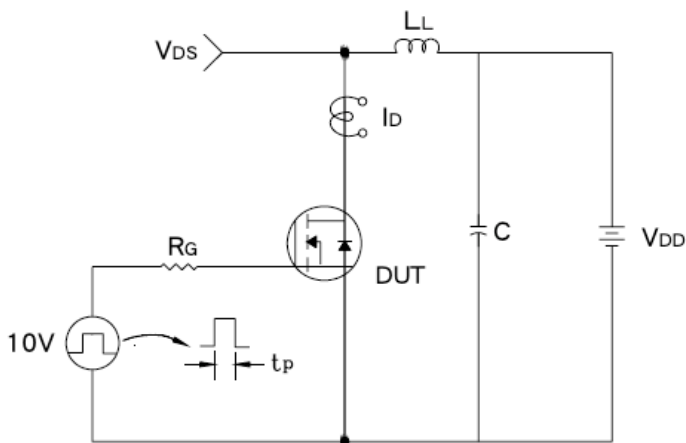
Gate Charge Test Circuit & Waveform



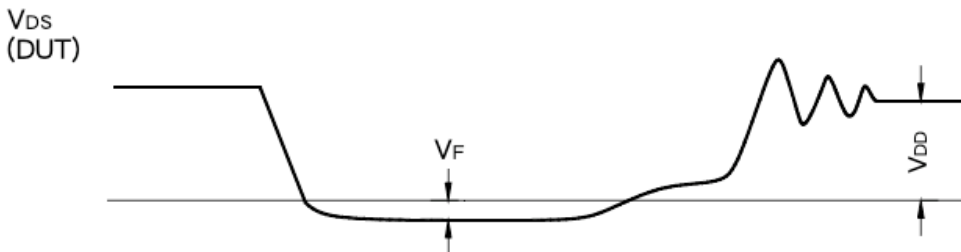
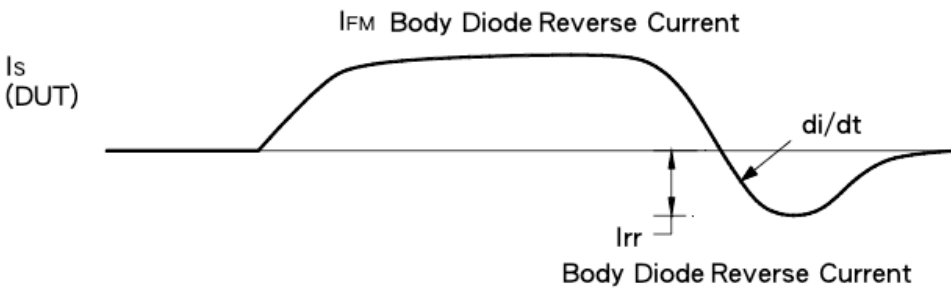
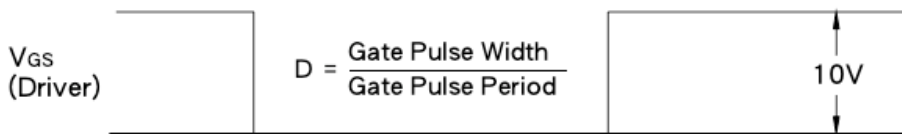
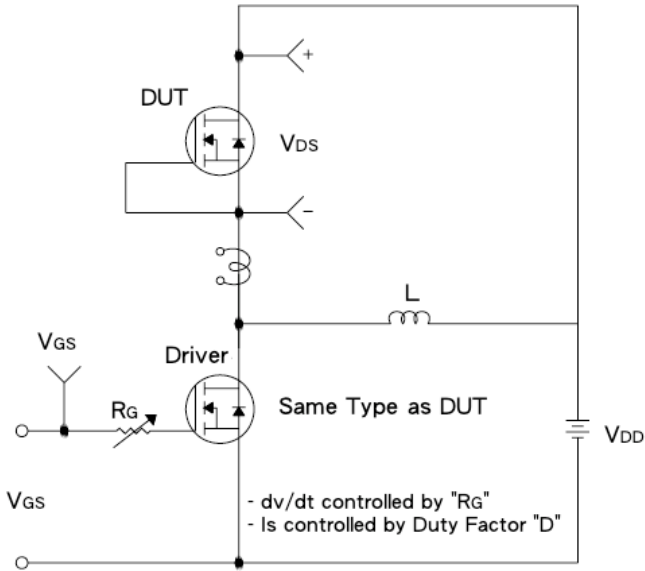
Resistive Switching Test Circuit & Waveform



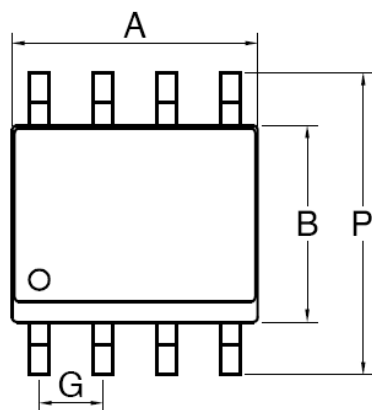
E_{AS} Test Circuit & Waveform



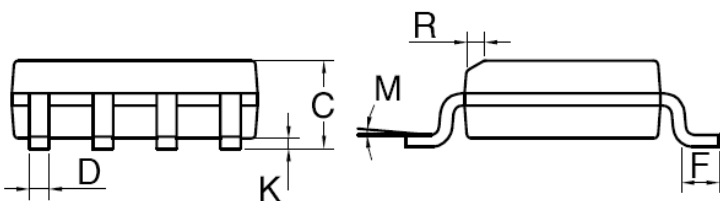
Diode Reverse Recovery Time Test Circuit & Waveform



SOP-8 Mechanical Drawing



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019





Preliminary

TSM1N45D

450V N-Channel Power MOSFET

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