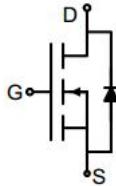
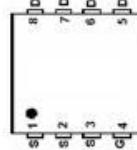


N-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The GT060N04D3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} 40V ● I_D (at $V_{GS} = 10V$) 40A ● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 6.5mΩ ● $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 10.5mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	 <p>Schematic diagram</p>  <p>pin assignment</p>  <p>DFN3X3-8L</p>
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Ordering Information

Device	Package	Marking	Packaging
GT060N04D3	DFN3X3-8L	GT060N04	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current (note1)	I_{DM}	160	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	24	W
Single pulse avalanche energy (note2)	E_{AS}	56	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	55	°C/W
Maximum Junction-to-Case	R_{thJC}	5.2	°C/W

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1	1.8	2.5	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$	--	5.5	6.5	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$	--	7.5	10.5	
Forward Transconductance	g_{FS}	$V_{\text{GS}} = 5\text{V}, I_D = 15\text{A}$	--	39	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 20\text{V}, f = 1.0\text{MHz}$	--	1297	--	pF
Output Capacitance	C_{oss}		--	363	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = 20\text{V}, I_D = 30\text{A}, V_{\text{GS}} = 10\text{V}$	--	32	--	nC
Gate-Source Charge	Q_{gs}		--	7	--	
Gate-Drain Charge	Q_{gd}		--	3	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 20\text{V}, I_D = 30\text{A}, R_G = 1.6\Omega$	--	6.5	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	21	--	
Turn-off Fall Time	t_f		--	3	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	40	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 30\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 30\text{A}, V_{\text{GS}} = 0\text{V}$ $dI/dt = 100\text{A}/\mu\text{s}$	--	16	--	nC
Reverse Recovery Time	T_{rr}		--	28	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J=25^\circ\text{C}$, $V_{\text{DD}}=40\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$
3. Identical low side and high side switch with identical R_G

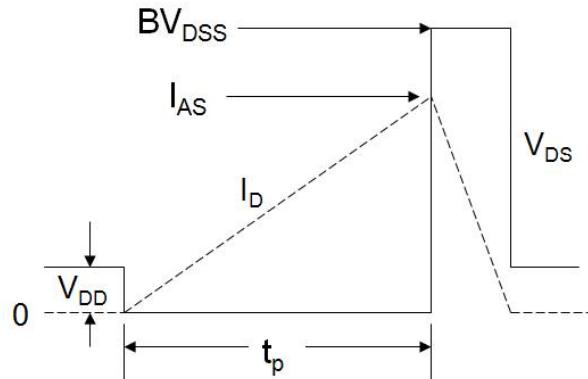
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

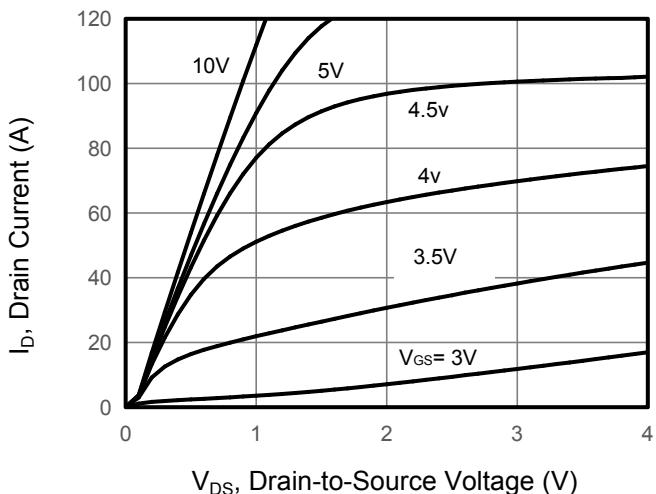


Figure 2. Transfer Characteristics

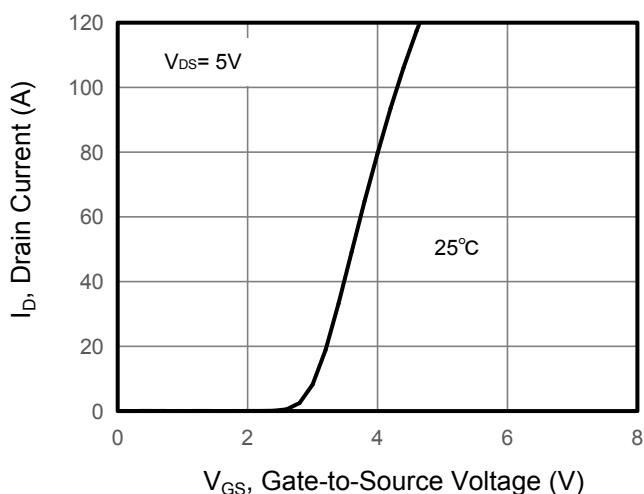


Figure 3. Drain Source On Resistance

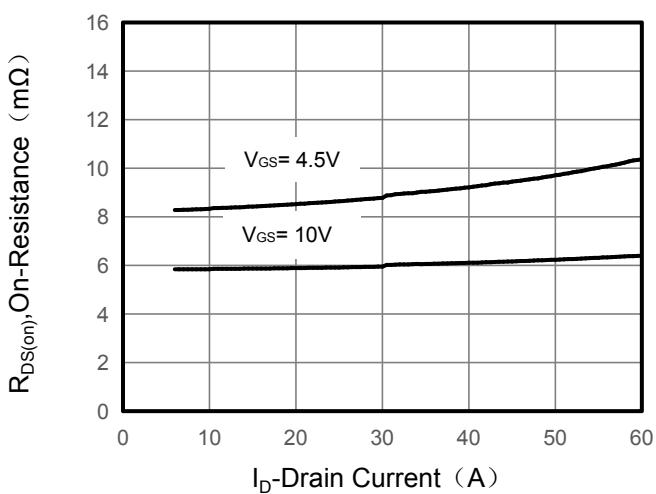


Figure 4. Gate Charge

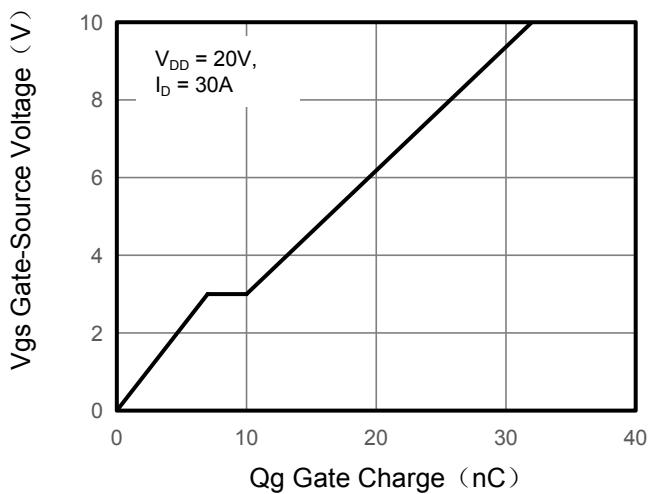


Figure 5. Capacitance

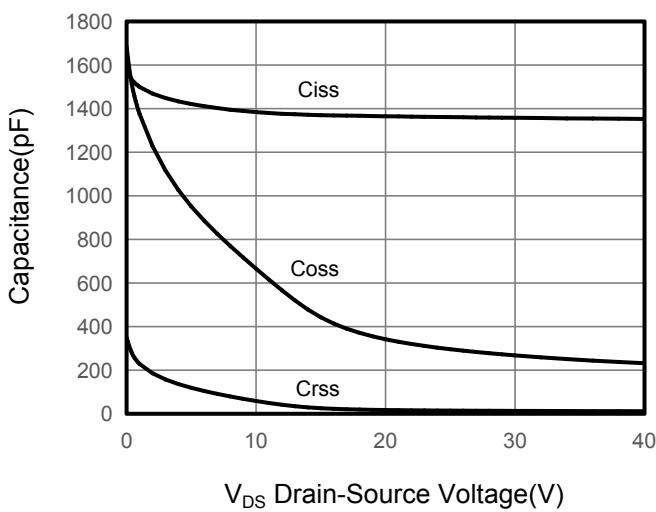
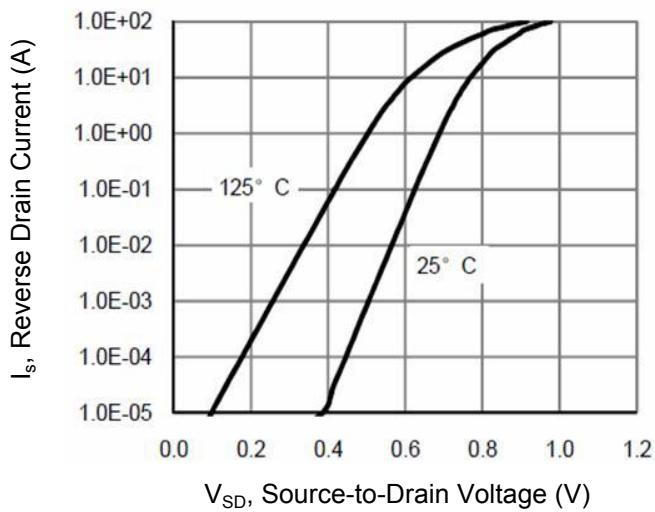


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

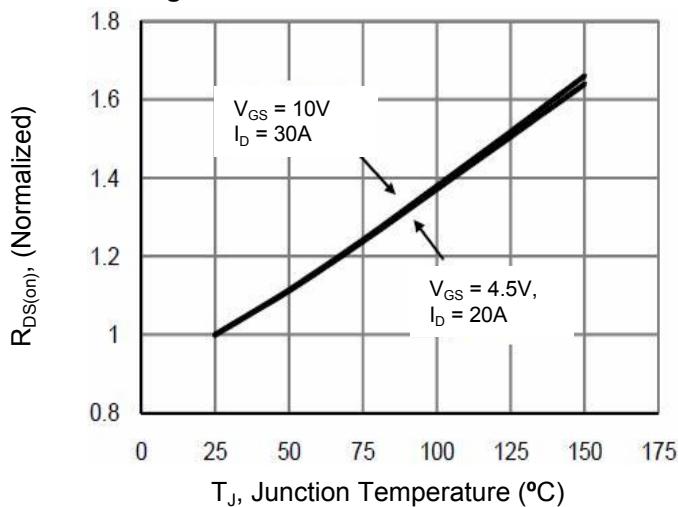


Figure 8. Safe Operation Area

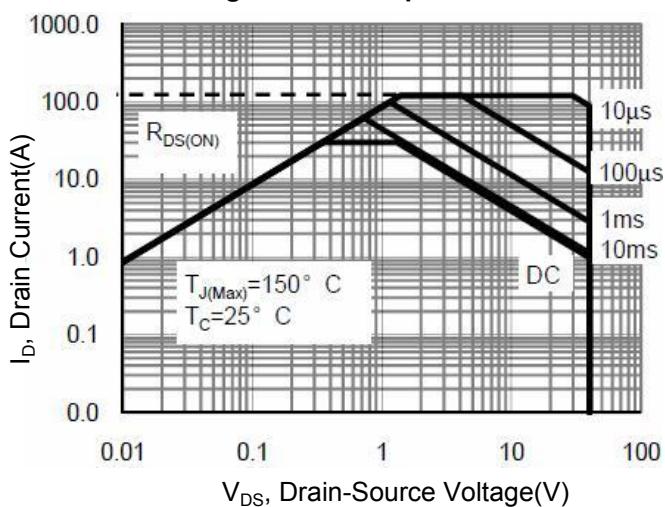
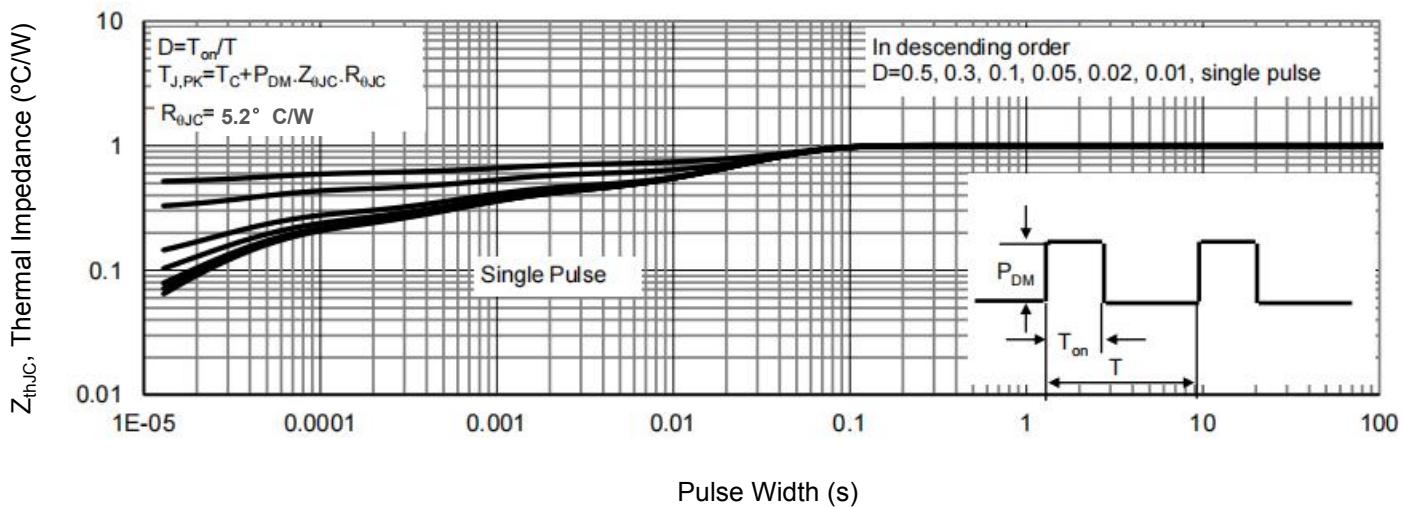
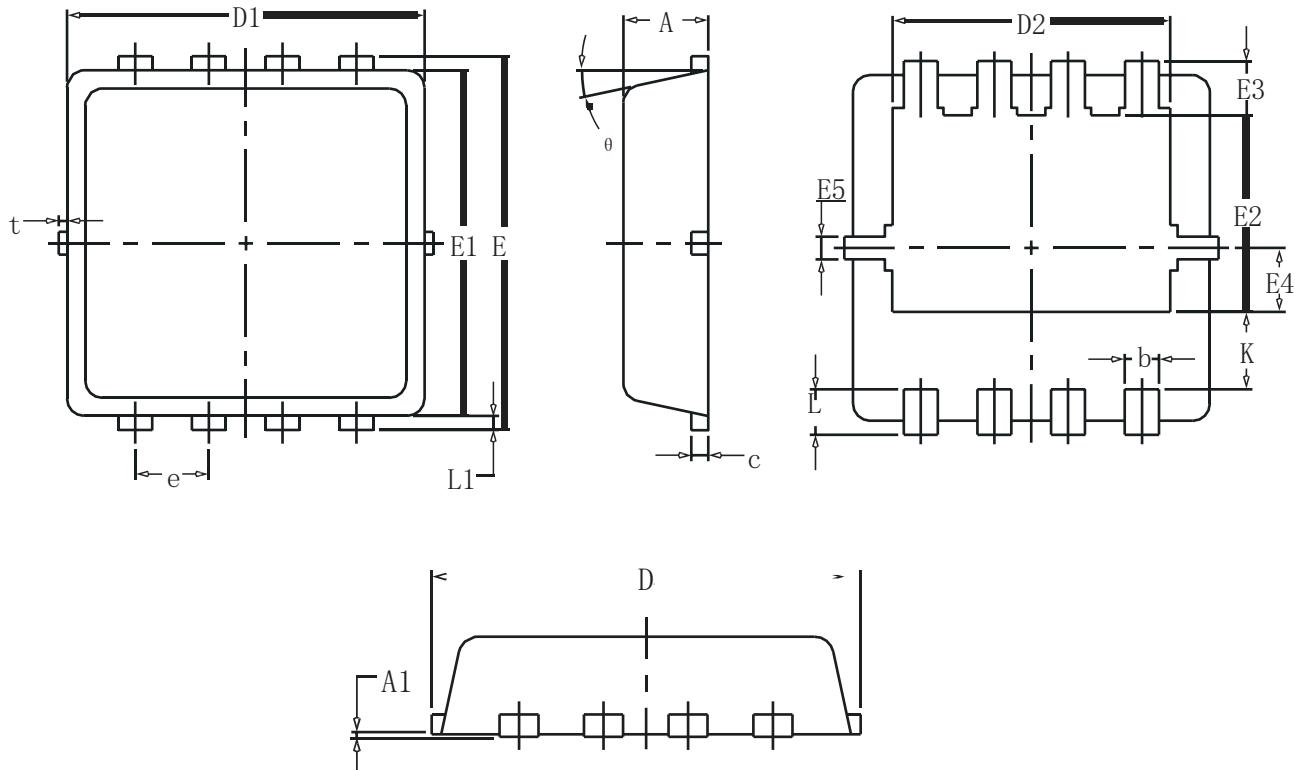


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN3x3-8L Package Information

SYMBOL	COMMON		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°