PCT2075

I²C-bus Fm+, 1 °C accuracy, digital temperature sensor and thermal watchdog

Rev. 10 — 20 November 2017 Product data sheet

1. General description

The PCT2075 is a temperature-to-digital converter featuring ±1 °C accuracy over −25 °C to +100 °C range. It uses an on-chip band gap temperature sensor and Sigma-Delta A-to-D conversion technique with an overtemperature detection output that is a drop-in replacement for other LM75 series thermal sensors. The device contains a number of data registers: Configuration register (Conf) to store the device settings such as device operation mode, OS operation mode, OS polarity and OS fault queue; temperature register (Temp) to store the digital temp reading, set-point registers (Tos and Thyst) to store programmable overtemperature shutdown and hysteresis limits, and programmable temperature sensor sampling time Tidle, that can be communicated by a controller via the 2-wire serial I²C-bus Fast-mode Plus interface.

The PCT2075 also includes an open-drain output (OS) which becomes active when the temperature exceeds the programmed limits. The OS output operates in either of two selectable modes: OS comparator mode or OS interrupt mode. Its active state can be selected as either HIGH or LOW. The fault queue that defines the number of consecutive faults in order to activate the OS output is programmable as well as the set-point limits.

The PCT2075 can be configured for different operation conditions. It can be set in normal mode to periodically monitor the ambient temperature, or in shut-down mode to minimize power consumption.

The temperature register always stores an 11-bit two's complement data, giving a temperature resolution of 0.125 °C. This high temperature resolution is particularly useful in applications of measuring precisely the thermal drift or runaway. When the device is accessed the conversion in process is not interrupted (that is, the I²C-bus section is totally independent of the Sigma-Delta converter section) and accessing the device continuously without waiting at least one conversion time between communications will not prevent the device from updating the Temp register with a new conversion result. The new conversion result is available immediately after the Temp register is updated. It is also possible to read just one of the temperature register bytes without lock-up.

The PCT2075 powers up in the normal operation mode with the OS in comparator mode, temperature threshold of 80 °C and hysteresis of 75 °C, so that it can be used as a stand-alone thermostat with those pre-defined temperature set points. The default set points can be modified during manufacture and ordered under custom part number.

There are three selectable logic address pins with three logic states so that 27 8-pin devices or three 6-pin devices can be connected on the same bus without address conflict.

2. Features and benefits

- Pin-for-pin replacement for LM75 series but allows up to 27 devices on the bus
- Power supply range from 2.7 V to 5.5 V
- Temperatures range from −55 °C to +125 °C
- Frequency range 20 kHz to 1 MHz with SMBus time-out to prevent hanging up the bus
- 1 MHz Fast-mode Plus 30 mA SDA drive allows more devices on the same bus but is backward compatible to Fast-mode and Standard-mode
- 11-bit ADC that offers a temperature resolution of 0.125 °C
- Temperature accuracy of:
  - ±1 °C (max.) from −25 °C to +100 °C
  - ±2 °C (max.) from −55 °C to +125 °C
- Programmable temperature threshold and hysteresis set points during operation
- Supply current of <1.0 μA in shut-down mode for power conservation
- Stand-alone operation as thermostat at power-up
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Small 8-pin package types: SO8, TSSOP8 and 2 mm × 3 mm HWSON8
- Small 6-pin package type: TSOP6

3. Applications

- System thermal management
- Personal computers
- Electronics equipment
- Industrial controllers
- Cooling system: turn on when the temperature is higher (hotter) than -5°C; turn off when the temperature is below -10°C

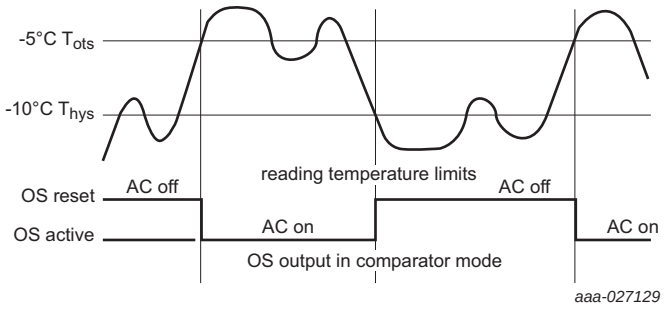


Fig 1. Cooling system using custom part PCT2075GV/N005

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCT2075D	PCT2075	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCT2075DP	P2075	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCT2075TP	075	HWSON8	plastic thermal enhanced very very thin small outline package; no leads; 8 terminals, 2 × 3 × 0.8 mm	SOT1069-2
PCT2075GV	20x[1]	TSOP6	plastic thin small outline package; 6 leads	SOT1353-1
PCT2075GV/N005[2]	05x[1]	TSOP6	plastic thin small outline package; 6 leads	SOT1353-1
PCT2075GV/P110[3]	10x[1]	TSOP6	plastic thin small outline package; 6 leads	SOT1353-1

[1] 'x' changes depending on the assembly work week 1 through 5

[2] PCT2075GV/N005 is a custom part with Tos = −5 °C and Thyst = −10 °C

[3] PCT2075GV/P110 is a custom part with Tos = 110 °C and Thyst = 105 °C

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCT2075D	PCT2075D,118	SO8	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = −55 °C to +125 °C
PCT2075DP	PCT2075DP,118	TSSOP8	Reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = −55 °C to +125 °C
PCT2075TP	PCT2075TP,147	HWSON8	Reel 7" Q2/T3 *standard mark	4000	T_{amb} = −55 °C to +125 °C
PCT2075GV	PCT2075GVJ	TSOP6	Reel 13" Q1/T1 *standard mark SMD	5000	T_{amb} = −55 °C to +125 °C
PCT2075GV	PCT2075GVX	TSOP6	Reel 7" Q1/T1 *standard mark SMD	3000	T_{amb} = −55 °C to +125 °C
PCT2075GV/N005	PCT2075GV/N005X	TSOP6	Reel 7" Q1/T1 *standard mark SMD	3000	T_{amb} = −55 °C to +125 °C
PCT2075GV/P110	PCT2075GV/P110X	TSOP6	Reel 7" Q1/T1 *standard mark SMD	3000	T_{amb} = −55 °C to +125 °C

5. Block diagram

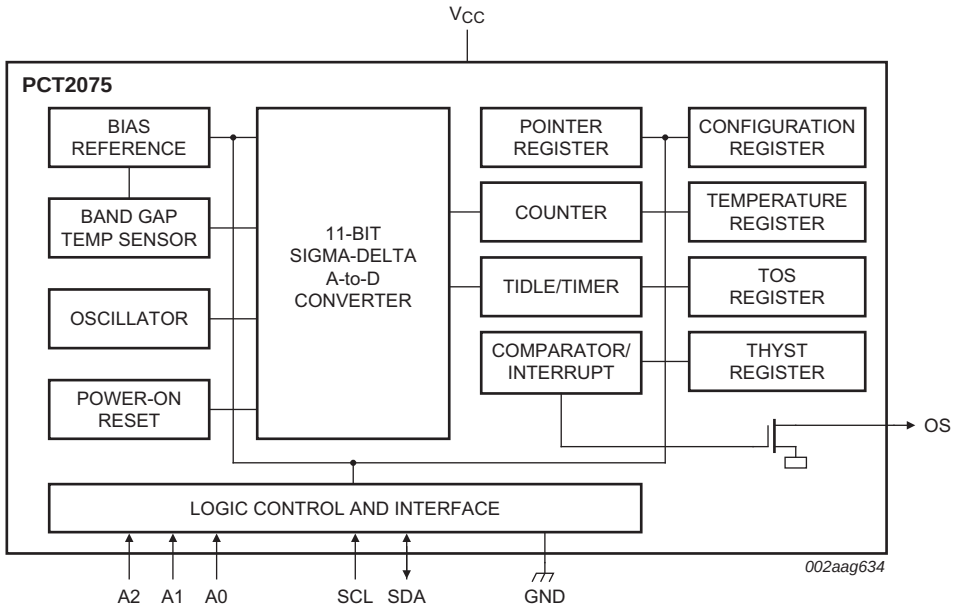


Fig 2. Block diagram of PCT2075

6. Pinning information

6.1 Pinning

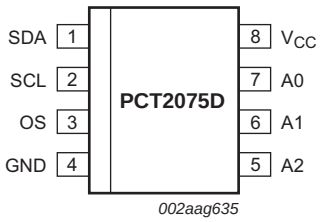


Fig 3. Pin configuration for SO8

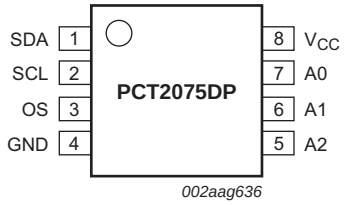


Fig 4. Pin configuration for TSSOP8

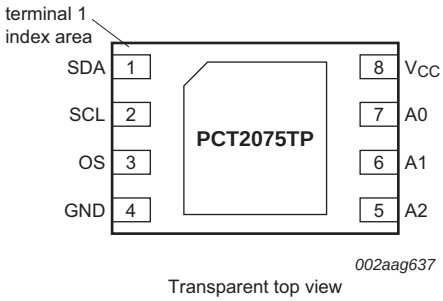


Fig 5. Pin configuration for HWSON8

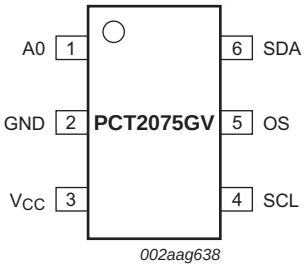


Fig 6. Pin configuration for TSOP6

6.2 Pin description

Table 3. Pin description for SO8, TSSOP8 and HWSON8

Symbol	Pin	Description
SDA	1	Digital I/O. I²C-bus serial bidirectional data line; open-drain.
SCL	2	Digital input. I²C-bus serial clock input.
OS	3	Overtemp Shutdown output; open-drain.
GND	4[1]	Ground. To be connected to the system ground.
A2	5	Digital input. User-defined address bit 2.
A1	6	Digital input. User-defined address bit 1.
A0	7	Digital input. User-defined address bit 0.
V_{CC}	8	Power supply.

[1] HWSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad should be soldered to the board using a corresponding thermal pad on the board, and for proper head conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

Table 4. Pin description for TSOP6

Symbol	Pin	Description
A0	1	Digital input. User-defined address bit 0.
GND	2	Ground. To be connected to the system ground.
V_{CC}	3	Power supply.
SCL	4	Digital input. I²C-bus serial clock input.
OS	5	Overtemp Shutdown output; open-drain.
SDA	6	Digital I/O. I²C-bus serial bidirectional data line; open-drain.

7. Functional description

7.1 General operation

The PCT2075 uses the on-chip band gap sensor to measure the device temperature with the resolution of 0.125 °C and stores the 11-bit two's complement digital data, resulted from 11-bit A-to-D conversion, into the device Temp register. This Temp register can be read at any time by a controller on the I²C-bus. Reading temperature data does not affect the conversion in progress during the read operation.

The PCT2075 can be set to operate in either mode: normal or shutdown. In normal operation mode, the temp-to-digital conversion is executed every 100 ms or other programmed value and the Temp register is updated at the end of each conversion. During each 'conversion period' (T_{conv}) of about 100 ms, the device takes only about 28 ms, called 'temperature conversion time' ($t_{conv(T)}$), to complete a temperature-to-data conversion and then becomes idle for the time remaining in the period. This feature is implemented to significantly reduce the device power dissipation.

In shutdown mode, the device becomes idle, data conversion is disabled and the Temp register holds the latest result; however, the device I²C-bus interface is still active and register write/read operation can be performed. The device operation mode is controllable by programming bit B0 of the configuration register. The temperature conversion is initiated when the device is powered-up or put back into normal mode from shutdown.

In addition, at the end of each conversion in normal mode, the temperature data (or Temp) in the Temp register is automatically compared with the overtemperature shutdown threshold data (or T_{ots}) stored in the Tos register, and the hysteresis data (or T_{hys}) stored in the Thyst register, in order to set the state of the device OS output accordingly. The device Tos and Thyst registers are write/read capable, and both operate with 9-bit two's complement digital data. To match with this 9-bit operation, the Temp register uses only the 9 MSB bits of its 11-bit data for the comparison. T_{ots} must always be higher than T_{hys}.

The way that the OS output responds to the comparison operation depends upon the OS operation mode selected by configuration bit B1, and the user-defined fault queue defined by configuration bits B3 and B4.

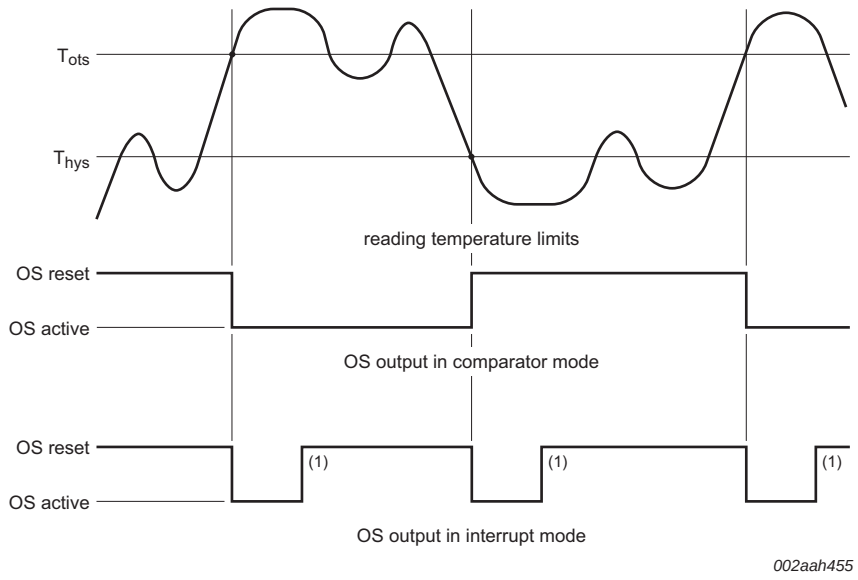
In OS comparator mode, the OS output behaves like a thermostat. It becomes active when the Temp exceeds the T_{ots}, and is reset when the Temp drops below the T_{hys}. Reading the device registers or putting the device into shutdown does not change the state of the OS output. The OS output in this case can be used to control cooling fans or thermal switches.

In OS interrupt mode, the OS output is used for thermal interruption. When the device is powered-up, the OS output is first activated only when the Temp exceeds the T_{ots}, then it remains active indefinitely until being reset by a read of any register. Once the OS output has been activated by crossing T_{ots} and then reset, it can be activated again only when the Temp drops below the T_{hys}; then again, it remains active indefinitely until being reset by a read of any register. The OS interrupt operation would be continued in this sequence: T_{ots} trip, Reset, T_{hys} trip, Reset, T_{ots} trip, Reset, T_{hys} trip, Reset, etc. Putting the device into the shutdown mode by setting the bit 0 of the configuration register also resets the OS output.

In both cases, comparator mode and interrupt mode, the OS output is activated only if a number of consecutive faults, defined by the device fault queue, has been met. The fault queue is programmable and stored in the two bits, B3 and B4, of the Configuration register. Also, the OS output active state is selectable as HIGH or LOW by setting accordingly the configuration register bit B2.

At power-up, the PCT2075 is put into normal operation mode in OS comparator mode, the T_{ots} is set to 80 °C, the T_{hys} is set to 75 °C, the OS active state is selected LOW and the fault queue is equal to 1. The temp reading data is 0 °C and not updated until the first conversion is completed in about 28 ms. The default T_{ots} and T_{hys} is set at the factory and can be modified on custom part number.

The OS response to the temperature is illustrated in Figure 7.



(1) OS is reset by either reading register or putting the device in shutdown mode. It is assumed that the fault queue is met at each T_{ots} and T_{hys} crossing point.

Fig 7. OS response to temperature

7.2 I²C-bus serial interface

The device can be connected to a compatible 2-wire serial interface Fast-mode Plus I²C-bus as a slave device under the control of a controller or master device, using two device terminals, SCL and SDA. The controller must provide the SCL clock signal and write/read data to/from the device through the SDA terminal. Notice that if the I²C-bus common pull-up resistors have not been installed as required for I²C-bus, then an external pull-up resistor, about 1.5 kΩ, is needed for each of these two terminals. The bus communication protocols are described in Section 7.10.

7.2.1 Bus fault time-out

If the SDA line is held LOW for longer than t_{to} (25 ms minimum; guaranteed at 35 ms maximum), the device resets to the idle state (SDA released) and waits for a new START condition. This ensures that the device never hangs up the bus if there are conflicts in the transmission sequence. The bus fault time-out can be disabled during manufacture and shipped under custom part number.

7.3 Slave address

To communicate with the device, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation. The device features three address pins to allow up to 27 devices to be addressed on a single bus interface. Table 5 describes the pin logic levels used to properly connect up to 27 8-pin devices. Table 6 describes the pin logic levels used to properly connect up to three 6-pin devices.
'1' indicates the pin is connected to the supply (V_{CC}); '0' indicates the pin is connected to GND; 'Float' indicates the pin is left unconnected. The states of pins A0/A1/A2 are sampled only at power-up. After sampling the address is latched to minimize power dissipation associated with detection.

Table 5. PCT2075 address table (SO8, TSSOP8, HWSON8 packages)

No.	Address pin coding			Slave address
	A2	A1	A0	
1	0	0	0	1001 000
2	0	0	1	1001 001
3	0	1	0	1001 010
4	0	1	1	1001 011
5	1	0	0	1001 100
6	1	0	1	1001 101
7	1	1	0	1001 110
8	1	1	1	1001 111
9	floating	0	0	1110 000
10	floating	0	floating	1110 001
11	floating	0	1	1110 010
12	floating	1	0	1110 011
13	floating	1	floating	1110 100
14	floating	1	1	1110 101
15	floating	floating	0	1110 110
16	floating	floating	1	1110 111
17	0	floating	0	0101 000
18	0	floating	1	0101 001
19	1	floating	0	0101 010
20	1	floating	1	0101 011
21	0	0	floating	0101 100
22	0	1	floating	0101 101
23	1	0	floating	0101 110

Table 5. PCT2075 address table (SO8, TSSOP8, HWSON8 packages) *…continued*

No.	Address pin coding			Slave address
	A2	A1	A0	
24	1	1	floating	0101 111
25	0	floating	floating	0110 101
26	1	floating	floating	0110 110
27	floating	floating	floating	0110 111

Table 6. PCT2075 address table (TSOP6 package)

No.	Address pin coding	Slave address
	A0	
1	float	1001 000
2	0	1001 001
3	1	1001 010

7.4 Register list

The PCT2075 contains four data registers beside the pointer register as listed in Table 7. The pointer value, read/write capability and default content at power-up of the registers are also shown in Table 7.

Table 7. Register table

Register name	Pointer value	R/W	POR state	Description
Conf	01h	R/W	00h	Configuration register: contains a single 8-bit data byte; to set the device operating condition; default = 0.
Temp	00h	read only	0000h	Temperature register: contains two 8-bit data bytes; to store the measured Temp data.
Tos	03h	R/W	5000h	Overtemperature shutdown threshold register: contains two 8-bit data bytes; to store the overtemperature shutdown T_{ots} limit; default = 80 °C.
			6E00h	Default = 110°C for PCT2075GV/P110 only.
			FB00h	Default = -5°C for PCT2075GV/N005 only.
Thyst	02h	R/W	4B00h	Hysteresis register: contains two 8-bit data bytes; to store the hysteresis T_{hys} limit; default = 75 °C.
			6900h	Default = 105°C for PCT2075GV/P110 only.
			F600h	Default = -10°C for PCT2075GV/N005 only.
Tidle	04h	R/W	00h	Temperature conversion cycle default to 100 ms.

7.4.1 Pointer register

The Pointer register contains an 8-bit data byte, of which the three LSB bits represent the pointer value of the other five registers, and the other five MSB bits are equal to 0, as shown in Table 8 and Table 9. The Pointer register is not accessible to the user, but is used to select the data register for write/read operation by including the pointer data byte in the bus command.

Table 8. Pointer register

B7	B6	B5	B4	B3	B[2:0]
0	0	0	0	0	pointer value

Table 9. Pointer value

B2	B1	B0	Selected register
0	0	0	Temperature register (Temp)
0	0	1	Configuration register (Conf)
0	1	0	Hysteresis register (Thyst)
0	1	1	Overtemperature shutdown register (Tos)
1	0	0	Idle register (Tidle)

Because the Pointer value is latched into the Pointer register when the bus command (which includes the pointer byte) is executed, a read from the device may or may not include the pointer byte in the statement. To read again a register that has been recently read and the pointer has been preset, the pointer byte does not have to be included. To read a register that is different from the one that has been recently read, the pointer byte must be included. However, a write to the device must always include the pointer byte in the statement. The bus communication protocols are described in Section 7.10.

At power-up, the Pointer value is equal to 000b and the Temp register is selected; users can then read the Temp data without specifying the pointer byte.

Anything not shown in Table 9 is reserved and should not be used.

7.4.2 Configuration register

The Configuration register (Conf) is a write/read register and contains an 8-bit non-complement data byte that is used to configure the device for different operation conditions. Table 10 shows the bit assignments of this register.

Table 10. Conf register

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
B[7:5]	reserved	R/W	000*	unused; any value written to these bits does not affect operation
B[4:3]	OS_F_QUE[1:0]	R/W		OS fault queue programming
			00*	queue value = 1
			01	queue value = 2
			10	queue value = 4
			11	queue value = 6
B2	OS_POL	R/W		OS polarity selection
			0*	OS active LOW
			1	OS active HIGH
B1	OS_COMP_INT	R/W		OS operation mode selection
			0*	OS comparator
			1	OS interrupt
B0	SHUTDOWN	R/W		device operation mode selection
			0*	normal
			1	shutdown

7.4.3 Temperature register

The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in two's complement format with the resolution of 0.125 °C. Table 11 shows the bit arrangement of the Temp data in the data bytes.

Table 11. Temp register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X

When reading register Temp, all 16 bits of the two data bytes (MSByte and LSByte) are provided to the bus and should be all collected by the controller for a valid temperature reading. However, only the 11 most significant bits should be used, and the five least significant bits of the LSByte are zero and should be ignored. One of the ways to calculate the Temp value in °C from the 11-bit Temp data is:

1. If the Temp data MSByte bit D10 = 0, then the temperature is positive and Temp value (°C) = +(Temp data) × 0.125 °C.
2. If the Temp data MSByte bit D10 = 1, then the temperature is negative and Temp value (°C) = −(two's complement of Temp data) × 0.125 °C.

Examples of the Temp data and value are shown in Table 12.

Table 12. Temp register value

11-bit binary (two's complement)	Hexadecimal value	Decimal value	Value
011 1111 1000	3F8	1016	+127.000 °C
011 1111 0111	3F7	1015	+126.875 °C
011 1111 0001	3F1	1009	+126.125 °C
011 1110 1000	3E8	1000	+125.000 °C
000 1100 1000	0C8	200	+25.000 °C
000 0000 0001	001	1	+0.125 °C
000 0000 0000	000	0	0.000 °C
111 1111 1111	7FF	–1	–0.125 °C
111 0011 1000	738	–200	–25.000 °C
110 0100 1001	649	–439	–54.875 °C
110 0100 1000	648	–440	–55.000 °C

For 9-bit Temp data application in replacing the industry standard LM75, just use only 9 MSB bits of the two bytes and disregard 7 LSB of the LSByte. The 9-bit Temp data with 0.5 °C resolution of the device is defined exactly in the same way as for the standard LM75 and it is here similar to the Tos and Thyst registers.

A single byte read (MSByte) of the Temp register is allowed. Then the temperature resolution is 1.00 °C instead.

7.4.4 Overtemperature shutdown threshold (Tos) and hysteresis (Thyst) registers

These two registers, are write/read registers, and also called set-point registers. They are used to store the user-defined temperature limits, called overtemperature shutdown threshold (T_{ots}) and hysteresis temperature (T_{hys}), for the device watchdog operation. At the end of each conversion the Temp data is compared with the data stored in these two registers in order to set the state of the device OS output; see Section 7.1.

Each of the set-point registers contains two 8-bit data bytes consisting of one MSByte and one LSByte in the same format as the Temperature register. However, only 9 bits of the two bytes are used to store the set-point data in two's complement format with the resolution of 0.5 °C. Table 13 and Table 14 show the bit arrangement of the Tos data and Thyst data in the data bytes.

Notice that because only 9-bit data are used in the set-point registers, the device uses only the 9 MSB of the Temp data for data comparison.

Table 13. Tos register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

Table 14. Thyst register

MSByte								LSByte							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X

When a set-point register is read, all 16 bits are provided to the bus and must be collected by the controller for a valid temperature. However, only the 9 most significant bits should be used and the 7 LSB of the LSByte are equal to zero and should be ignored.

A single byte read of either Tos or Thyst is allowed.

Table 15 shows examples of the limit data and value.

Table 15. Tos and Thyst limit data and value

11-bit binary (two's complement)	Hexadecimal value	Decimal value	Value
0 1111 1010	0FA	250	+125.0 °C
0 0011 0010	032	50	+25.0 °C
0 0000 0001	001	1	+0.5 °C
0 0000 0000	000	0	0.0 °C
1 1111 1111	1FF	–1	–0.5 °C
1 1100 1110	1CE	–50	–25.0 °C
1 1001 0010	192	–110	–55.0 °C

7.4.5 Tidle register

For the device temperature sensor, the temperature is measured periodically to save power. When the temperature is being measured, the device burns approximately 70 μA active current. Since the ambient temperature changes slowly, it is unnecessary to let the temperature measurement continuously active. Instead, the device temperature sensor is set to idle for a user-specified time to save power after temperature measurement is done.

The Tidle register allows users to specify the sampling period to measure the temperature. The register is composed of 5-bit values TIDLE[4:0] at pointer address 04h. The values of TIDLE[7:5] are 'don't care' and have no effect on the temperature measurement period. The temperature measurement period can be calculated by TIDLE[4:0] × 100 ms. For example, if TIDLE[4:0] = 00001, the temperature sampling is '00001' × 100 ms = 100 ms. the temperature sensor allows a sampling period from 100 ms to 3.1 s by programming Tidle. If Tidle is set to '00000', it is treated the same as Tidle = '00001' and the temperature sensor measures temperature at 100 ms period.

Table 16. Tidle - Temperature idle register (address 04h) bit allocation

Temperature idle register contains the value of time in between temperature measurements. TIDLE[4:0] is the 5-bit Tidle value. Tidle × 100 ms is the temperature sampling period.

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	TIDLE[4]	TIDLE[3]	TIDLE[2]	TIDLE[1]	TIDLE[0]
Reset	-	-	-	0	0	0	0	1
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

The device temperature sensor powers up to measure temperature every 100 ms, with Tidle = 00001 by default. For the PCT2075 with 11-bit accuracy, the ADC conversion is about 28 ms. As a result, the PCT2075 is idle for (100 ms – 28 ms) = 72 ms between two temperature measurements.

7.5 OS output and polarity

The OS output is an open-drain output and its state represents results of the device watchdog operation as described in Section 7.1. In order to observe this output state, an external pull-up resistor is needed. The resistor should be as large as possible, up to 1.5 kΩ, to minimize the Temp reading error due to internal heating by the high OS sinking current.

The OS output active state can be selected as HIGH or LOW by programming bit B2 (OS_POL) of register Conf: setting bit OS_POL to logic 1 selects OS active HIGH and setting bit B2 to logic 0 sets OS active LOW. At power-up, bit OS_POL is equal to logic 0 and the OS active state is LOW.

7.6 OS comparator and interrupt modes

As described in Section 7.1, the device OS output responds to the result of the comparison between register Temp data and the programmed limits, in registers Tos and Thyst, in different ways depending on the selected OS mode: OS comparator or OS interrupt. The OS mode is selected by programming bit B1 (OS_COMP_INT) of register Conf: setting bit OS_COMP_INT to logic 1 selects the OS interrupt mode, and setting to logic 0 selects the OS comparator mode. At power-up, bit OS_COMP_INT is equal to logic 0 and the OS comparator is selected.

The main difference between the two modes is that in OS comparator mode, the OS output becomes active when Temp has exceeded T_{ots} and reset when Temp has dropped below T_{hys}, reading a register or putting the device into shutdown mode does not change the state of the OS output; while in OS interrupt mode, once it has been activated either by exceeding T_{ots} or dropping below T_{hys}, the OS output remains active indefinitely until reading a register, then the OS output is reset.

Temperature limits T_{ots} and T_{hys} must be selected so that $T_{ots} > T_{hys}$. Otherwise, the OS output state is undefined.

7.7 OS fault queue

Fault queue is defined as the number of faults that must occur consecutively to activate the OS output. It is provided to avoid false tripping due to noise. Because faults are determined at the end of data conversions, fault queue is also defined as the number of consecutive conversions returning a temperature trip. The value of fault queue is selectable by programming the two bits B4 and B3 (OS_F_QUE[1:0]) in register Conf. Notice that the programmed data and the fault queue value are not the same. Table 17 shows the one-to-one relationship between them. At power-up, fault queue data = 0 and fault queue value = 1.

Table 17. Fault queue table

Fault queue data		Fault queue value
OS_F_QUE[1]	**OS_F_QUE[0]**	**Decimal**
0	0	1
0	1	2
1	0	4
1	1	6

7.8 Shutdown mode

The device operation mode is selected by programming bit B0 (SHUTDOWN) of register Conf. Setting bit SHUTDOWN to logic 1 puts the device into shutdown mode. Resetting bit SHUTDOWN to logic 0 returns the device to normal mode.

In shutdown mode, the PCT2075 draws a small current of <1.0 μA and the power dissipation is minimized; the temperature conversion stops, but the I²C-bus interface remains active and register write/read operation can be performed. When the shutdown is set, the OS output is unchanged in comparator mode and reset in interrupt mode.

7.9 Power-up default and power-on reset

The PCT2075 always powers-up in its default state with:

- Normal operation mode
- OS comparator mode
- T_{ots} = 80 °C (or as specified for the custom part number)
- T_{hys} = 75 °C (or as specified for the custom part number)
- OS output active state is LOW
- Pointer value is logic 000 (Temp)
- SMBus time-out enabled (or as specified for the custom part number)

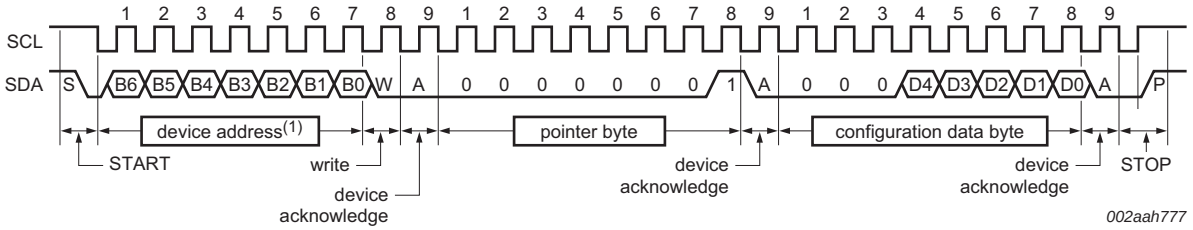
When the power supply voltage is dropped below the device power-on reset level of approximately 1.0 V (POR) for over 2 μs and then rises up again, the PCT2075 is reset to its default condition as listed above.

In some applications a higher or lower default T_{ots} and T_{hys} values or no SMBus time-out may be required. Please contact NXP for information on custom part number.

7.10 Protocols for writing and reading the registers

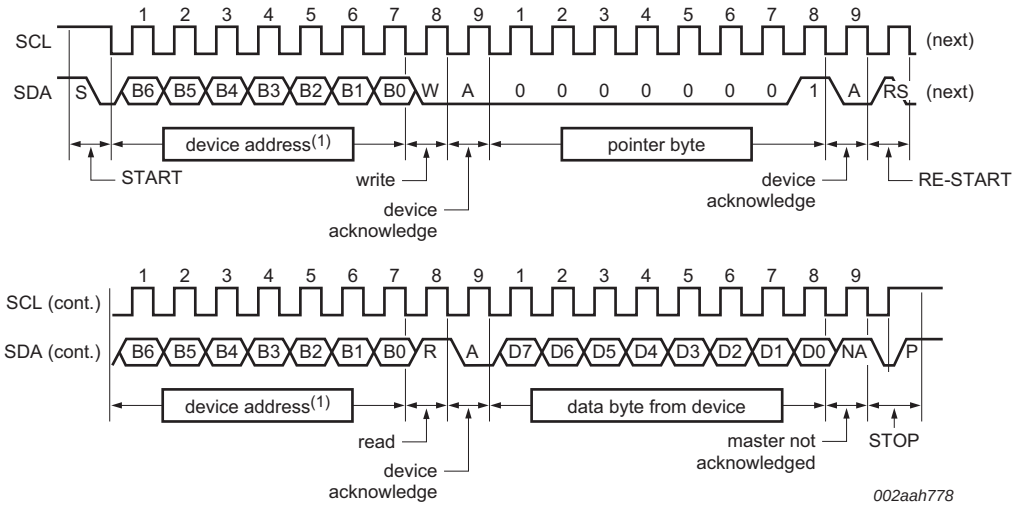
The communication between the host and the device must strictly follow the rules as defined by the I²C-bus management. The protocols for device register read/write operations are illustrated in Figure 8 to Figure 13 together with the following definitions:

1. Before a communication, the I²C-bus must be free or not busy. It means that the SCL and SDA lines must both be released by all devices on the bus, and they become HIGH by the bus pull-up resistors.
2. The host must provide SCL clock pulses necessary for the communication. Data is transferred in a sequence of 9 SCL clock pulses for every 8-bit data byte followed by 1-bit status of the acknowledgement.
3. During data transfer, except the START and STOP signals, the SDA signal must be stable while the SCL signal is HIGH. It means that the SDA signal can be changed only during the LOW duration of the SCL line.
4. S: START signal, initiated by the host to start a communication, the SDA goes from HIGH to LOW while the SCL is HIGH.
5. RS: RE-START signal, same as the START signal, to start a read command that follows a write command.
6. P: STOP signal, generated by the host to stop a communication, the SDA goes from LOW to HIGH while the SCL is HIGH. The bus becomes free thereafter.
7. W: write bit, when the write/read bit = LOW in a write command.
8. R: read bit, when the write/read bit = HIGH in a read command.
9. A: device acknowledge bit, returned by the device. It is LOW if the device works properly and HIGH if not. The host must release the SDA line during this period in order to give the device the control on the SDA line.
10. A': master acknowledge bit, not returned by the device, but set by the master or host in reading 2-byte data. During this clock period, the host must set the SDA line to LOW in order to notify the device that the first byte has been read for the device to provide the second byte onto the bus.
11. NA: Not Acknowledge bit. During this clock period, both the device and host release the SDA line at the end of a data transfer, the host is then enabled to generate the STOP signal.
12. In a write protocol, data is sent from the host to the device and the host controls the SDA line, except during the clock period when the device sends the device acknowledgement signal to the bus.
13. In a read protocol, data is sent to the bus by the device and the host must release the SDA line during the time that the device is providing data onto the bus and controlling the SDA line, except during the clock period when the master sends the master acknowledgement signal to the bus.
14. For best temperature accuracy both temperature bytes should be read as shown in Figure 12 and Figure 13, but for a quick less accurate check/reduce bus transmission then only one byte, the MSByte, needs to be read as shown in Figure 10.



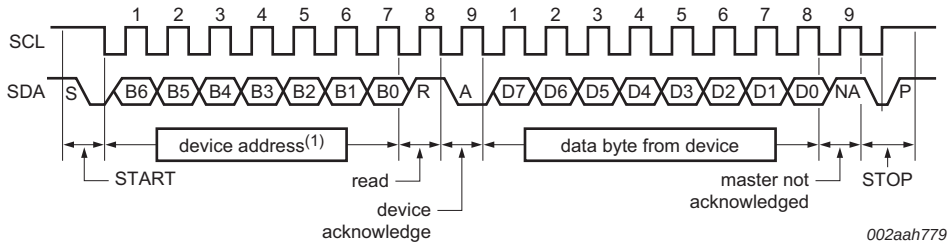
(1) See Table 5 or Table 6 for device address.

Fig 8. Write configuration register (1-byte data)



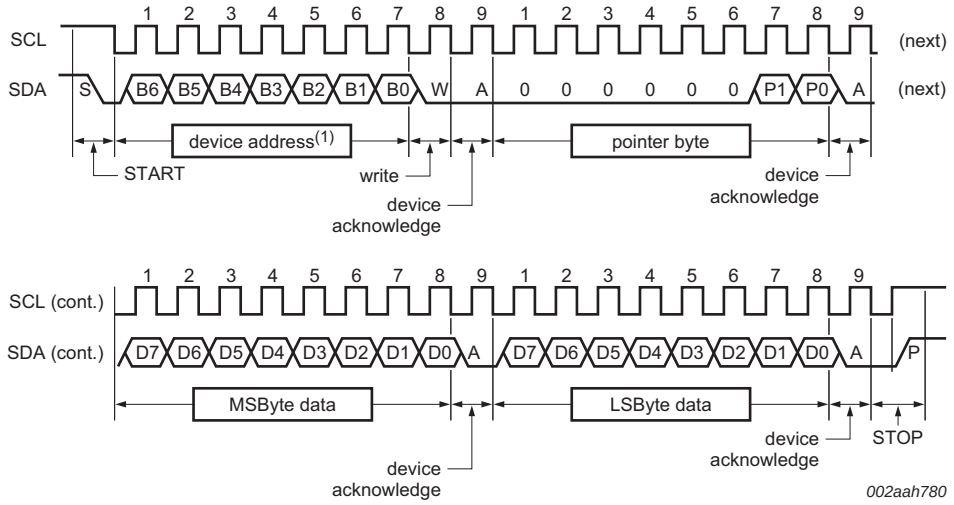
(1) See Table 5 or Table 6 for device address.

Fig 9. Read configuration register including pointer byte (1-byte data)



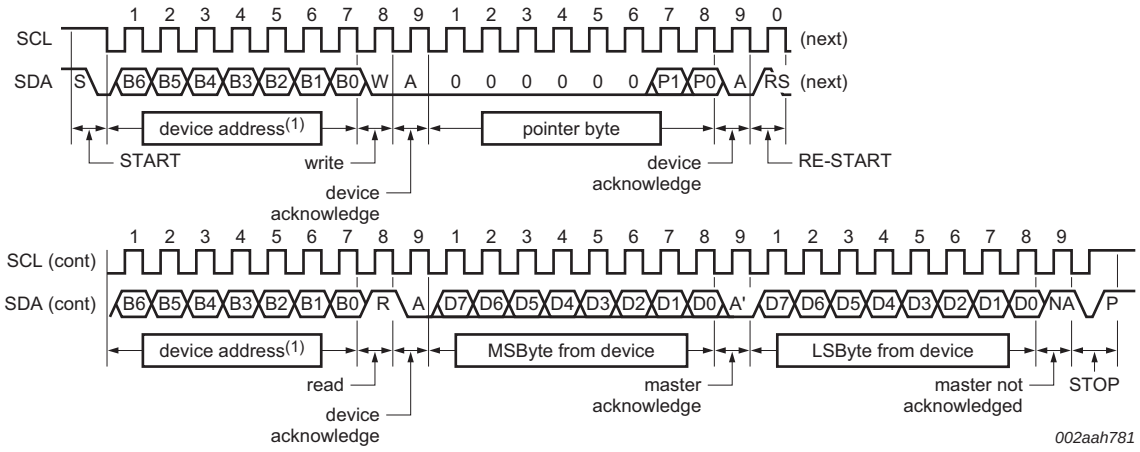
(1) See Table 5 or Table 6 for device address.

Fig 10. Read configuration or temp register with preset pointer (1-byte data)



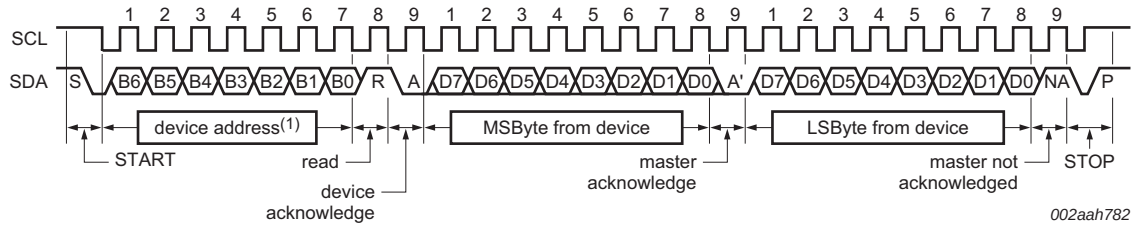
(1) See Table 5 or Table 6 for device address.

Fig 11. Write Tos or Thyst register (2-byte data)



(1) See Table 5 or Table 6 for device address.

Fig 12. Read Temp, Tos or Thyst register including pointer byte (2-byte data)



(1) See Table 5 or Table 6 for device address.

Fig 13. Read Temp, Tos or Thyst register with preset pointer (2-byte data)

8. Application design-in information

8.1 Typical application

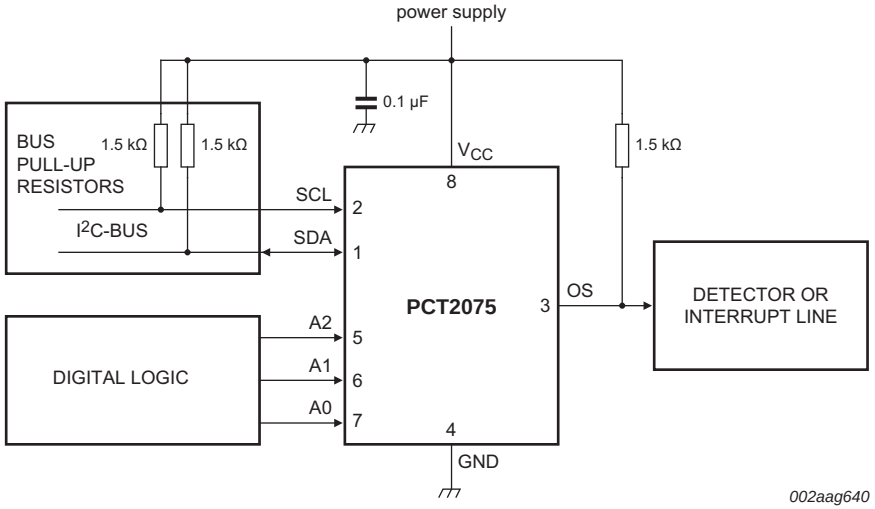


Fig 14. PCT2075 typical application

8.2 Temperature accuracy

Because the local channel of the temperature sensor measures its own die temperature that is transferred from its body, the temperature of the device body must be stabilized and saturated for it to provide the stable readings. Because the device operates at a low-power level, the thermal gradient of the device package has a minor effect on the measurement. The accuracy of the measurement is more dependent upon the definition of the environment temperature, which is affected by different factors: the printed-circuit board on which the device is mounted; the air flow contacting the device body (if the ambient air temperature and the printed-circuit board temperature are much different, then the measurement may not be stable because of the different thermal paths between the die and the environment). The stabilized temperature liquid of a thermal bath provides the best temperature environment when the device is completely dipped into it. A thermal probe with the device mounted inside a sealed-end metal tube located in consistent temperature air also provides a good method of temperature measurement.

8.3 Noise effect

The device design includes the implementation of basic features for a good noise immunity:

- The 50 ns low-pass filter on both the bus pins SCL and SDA;
- The hysteresis of the threshold voltages to the bus input signals SCL and SDA, about 500 mV minimum;
- All pins have ESD protection circuitry to prevent damage during electrical surges. The ESD protection on the address, OS, SCL and SDA pins it to ground. The latch-back based device breakdown voltage of address/OS is typically 11 V and SCL/SDA is typically 9.5 V at any supply voltage but varies over process and temperature. Since

there are no protection diodes from SCL or SDA to V_{CC}, the device will not hold the I^2C lines LOW when V_{CC} is not supplied and therefore allows continued I^2C-bus operation if the device is de-powered.

However, good layout practices and extra noise filters are recommended when the device is used in a very noisy environment:

- Use decoupling capacitors at V_{CC} pin.
- Keep the digital traces away from switching power supplies.
- Apply proper terminations for the long board traces.
- Add capacitors to the SCL and SDA lines to increase the low-pass filter characteristics.

9. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.3	+6.0	V
V_I	input voltage	at input pins		–0.3	+6.0	V
I_I	input current	at input pins		–5.0	+5.0	mA
$I_{O(sink)}$	output sink current	on pin OS		-	60	mA
V_O	output voltage	on pin OS		–0.3	+6.0	V
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature			-	150	°C

10. Recommended operating conditions

Table 19. Recommended operating characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			2.7	-	5.5	V
T_{amb}	ambient temperature			–55	-	+125	°C

11. Static characteristics

Table 20. Static characteristics

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −55 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{acc}	temperature accuracy	T_{amb} = −25 °C to +100 °C		−1	-	+1	°C
		T_{amb} = −55 °C to +125 °C		−2	-	+2	°C
T_{res}	temperature resolution	11-bit digital temp data		-	0.125	-	°C
$t_{conv(T)}$	temperature conversion time	normal mode		-	28	-	ms
T_{conv}	conversion period	normal mode		-	0.1	3.2	s
V_{POR}	power-on reset voltage			-	-	2.6	V
$I_{CC(AV)}$	average supply current	normal mode: I²C-bus inactive		-	125	300	µA
		normal mode: I²C-bus active; f_{SCL} = 1000 kHz		-	200	400	µA
		shutdown mode					
		T_{amb} = 25 °C		-	<0.1	-	µA
		T_{amb} = 85 °C		-	<1	-	µA
		T_{amb} = 125 °C		-	-	20	µA
V_{IH}	HIGH-level input voltage	digital pins (SCL, SDA, A2 to A0)		0.7 × V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	digital pins		−0.3	-	0.3 × V_{CC}	V
$V_{I(hys)}$	hysteresis of input voltage	SCL and SDA pins		-	300	-	mV
		A2, A1, A0 pins		-	150	-	mV
I_{IH}	HIGH-level input current	digital pins; V_I = V_{CC}					
		T_{amb} = 25 °C		-	<0.1	-	µA
		T_{amb} = 85 °C (PCT2075D, DP and TP only)		-	<1	-	µA
		T_{amb} = 85 °C (PCT2075GV only)		-	<2	-	µA
		T_{amb} = 125 °C (PCT2075D, DP and TP only)		-	-	10	µA
		T_{amb} = 125 °C (PCT2075GV only)		-	-	20	µA
I_{IL}	LOW-level input current	digital pins; V_I = 0 V		−1.0	-	+1.0	µA
V_{OL}	LOW-level output voltage	OS pin; I_{OL} = 20 mA		-	-	0.4	V
		SDA pin; I_{OL} = 20 mA		-	-	0.4	V
I_{LO}	output leakage current	SDA and OS pins; V_{OH} = V_{CC}		-	-	20	µA
N_{fault}	number of faults	programmable; conversions in overtemperature-shutdown fault queue		1	-	6	
T_B	overtemperature shutdown temperature	default value		-	80[2]	-	°C
T_{hys}	hysteresis temperature	default value		-	75[2]	-	°C
C_i	input capacitance	digital pins		-	20	-	pF

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Or values as specified for custom part number. See Table 7.

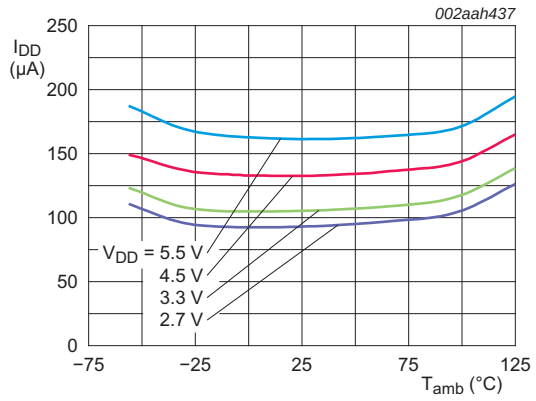


Fig 15. Average supply current versus temperature; I²C-bus inactive

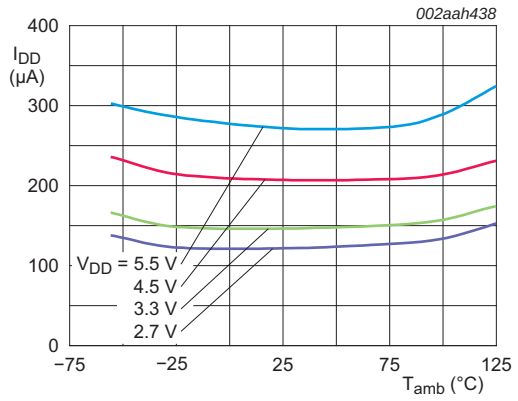


Fig 16. Average supply current versus temperature; I²C-bus active

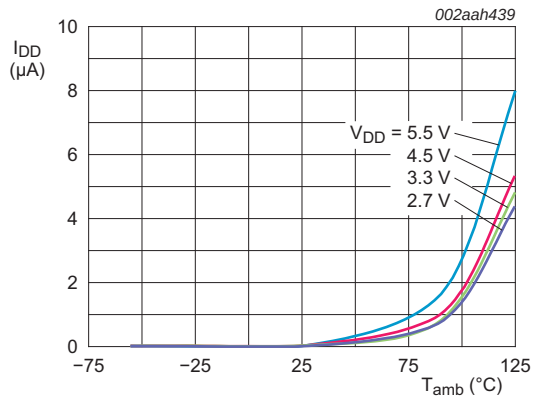


Fig 17. Shutdown mode supply current versus temperature

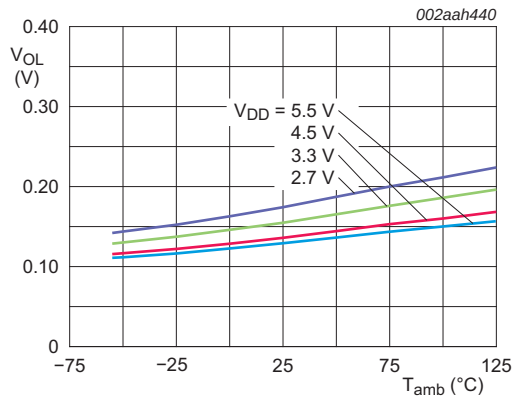


Fig 18. LOW-level output voltage on OS pin versus temperature; I_{OL} = 4 mA

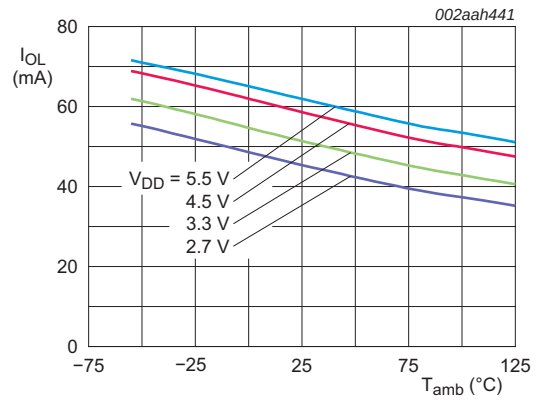


Fig 19. LOW-level output current on OS pin versus temperature; V_{OL} = 0.4 V

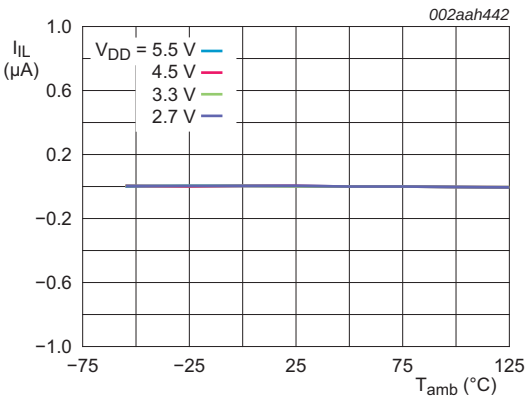


Fig 20. LOW-level input current versus temperature; digital pins

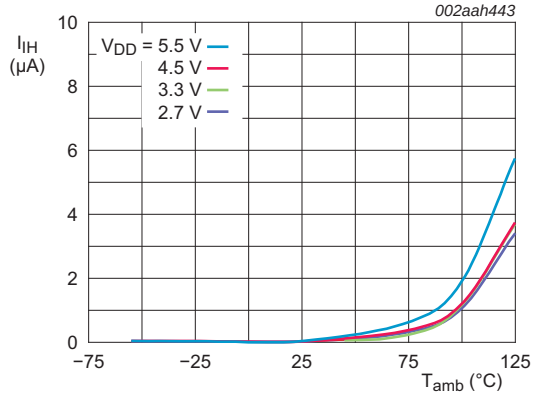


Fig 21. HIGH-level input current versus temperature; digital pins

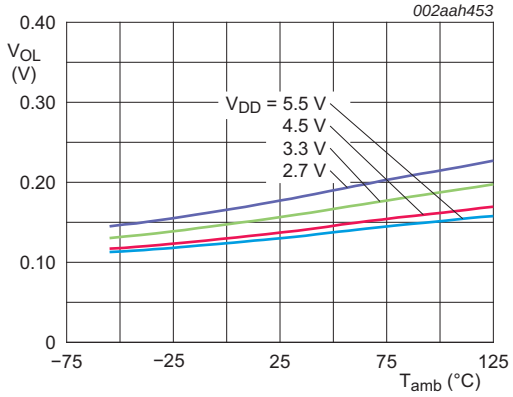


Fig 22. LOW-level output voltage on SDA pin versus temperature; I_{OL} = 20 mA

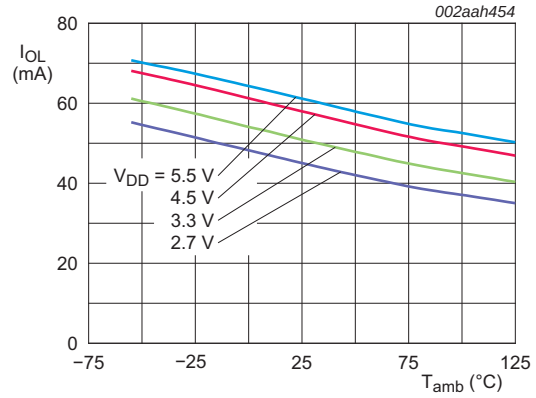


Fig 23. LOW-level output current on SDA pin versus temperature; V_{OL} = 0.4 V

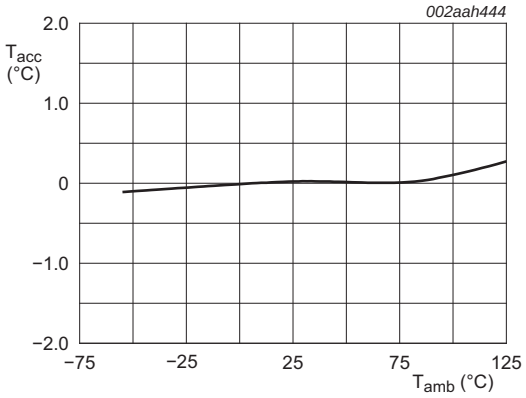


Fig 24. Temperature accuracy versus temperature; V_{CC} = 2.8 V to 5.5 V

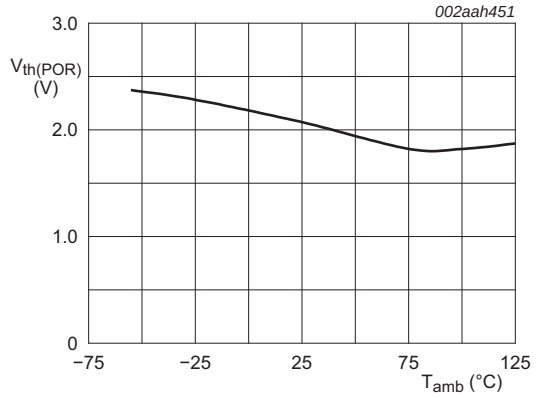


Fig 25. Power-on reset threshold voltage versus temperature; rising V_{CC}

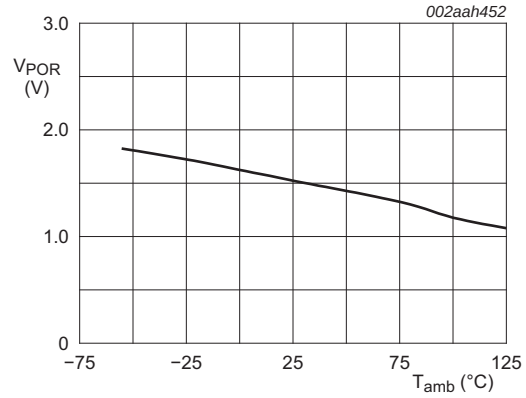


Fig 26. Power-on reset voltage versus temperature; falling V_{CC}

12. Dynamic characteristics

Table 21. I²C-bus interface dynamic characteristics[1]

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −55 °C to +125 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	see Figure 27		20	-	1000	kHz
t_{HIGH}	HIGH period of the SCL clock			0.26	-	-	µs
t_{LOW}	LOW period of the SCL clock			0.5	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			0.26	-	-	µs
$t_{SU;DAT}$	data set-up time			50	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.26	-	-	µs
t_f	fall time	SDA and OS outputs; C_L = 450 pF; I_{OL} = 30 mA		-	120	-	ns
$t_{to(SMBus)}$	SMBus time-out time		[2][3]	25	-	35	ms

[1] These specifications are guaranteed by design and not tested in production.

[2] This is the SDA time LOW for reset of serial interface.

[3] Holding the SDA line LOW for a time greater than t_{to} causes the device to reset SDA to the idle state of the serial bus communication (SDA set HIGH).

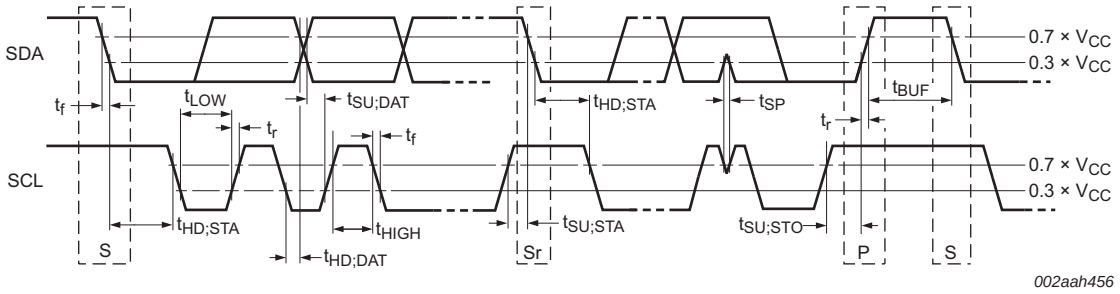
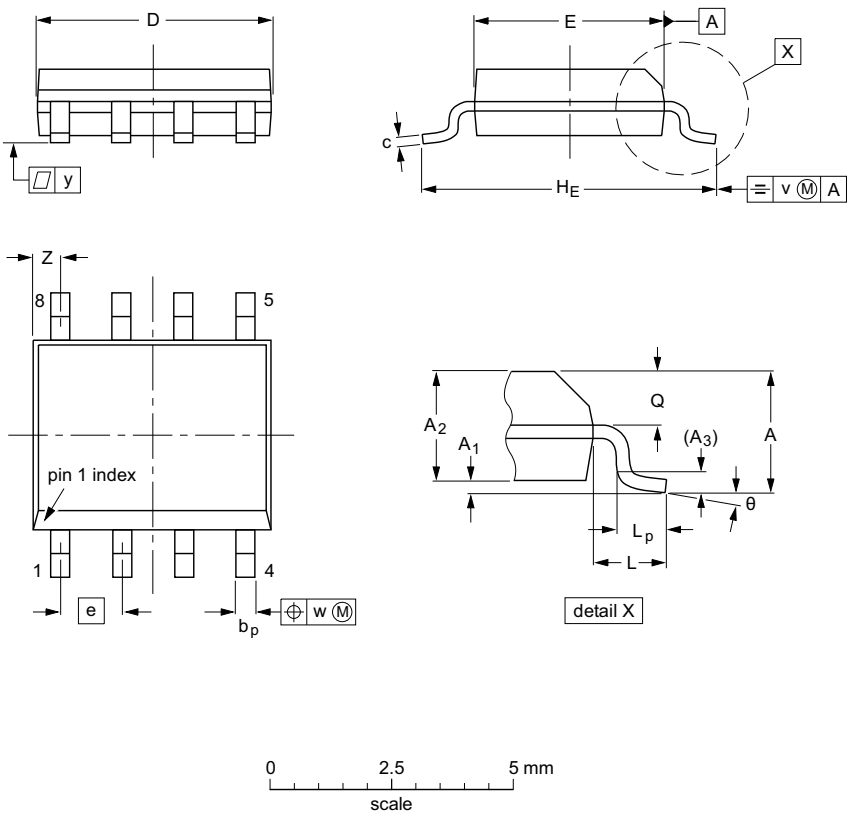


Fig 27. Timing diagram

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

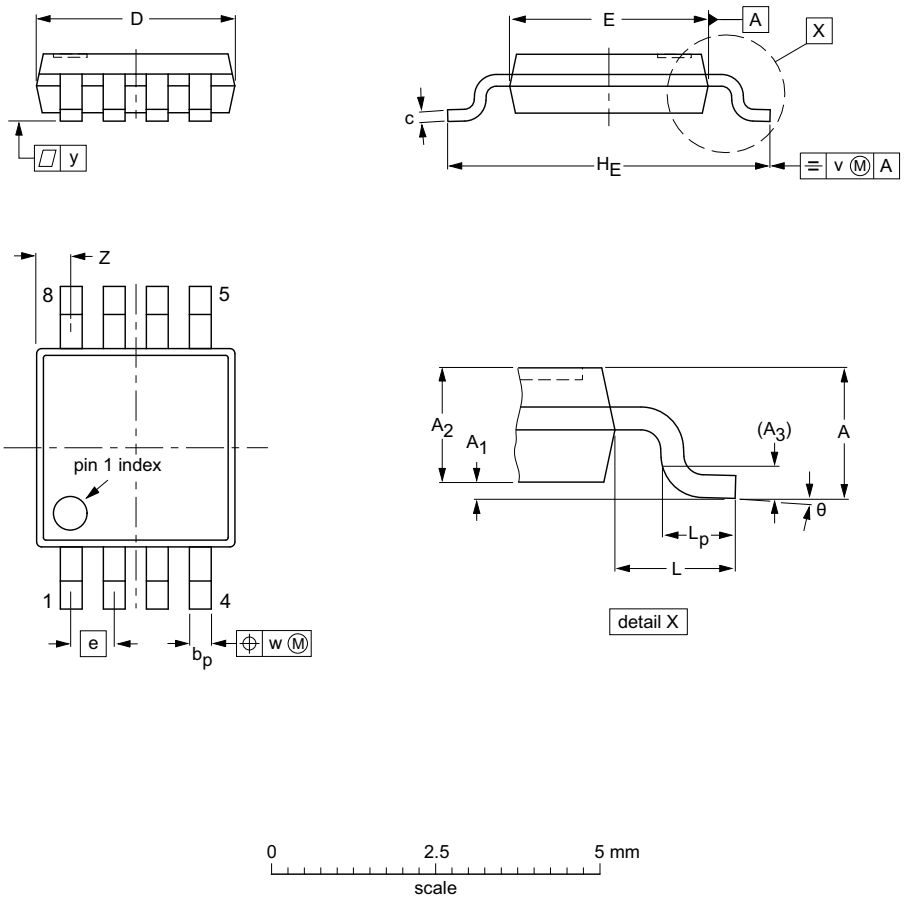
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 28. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

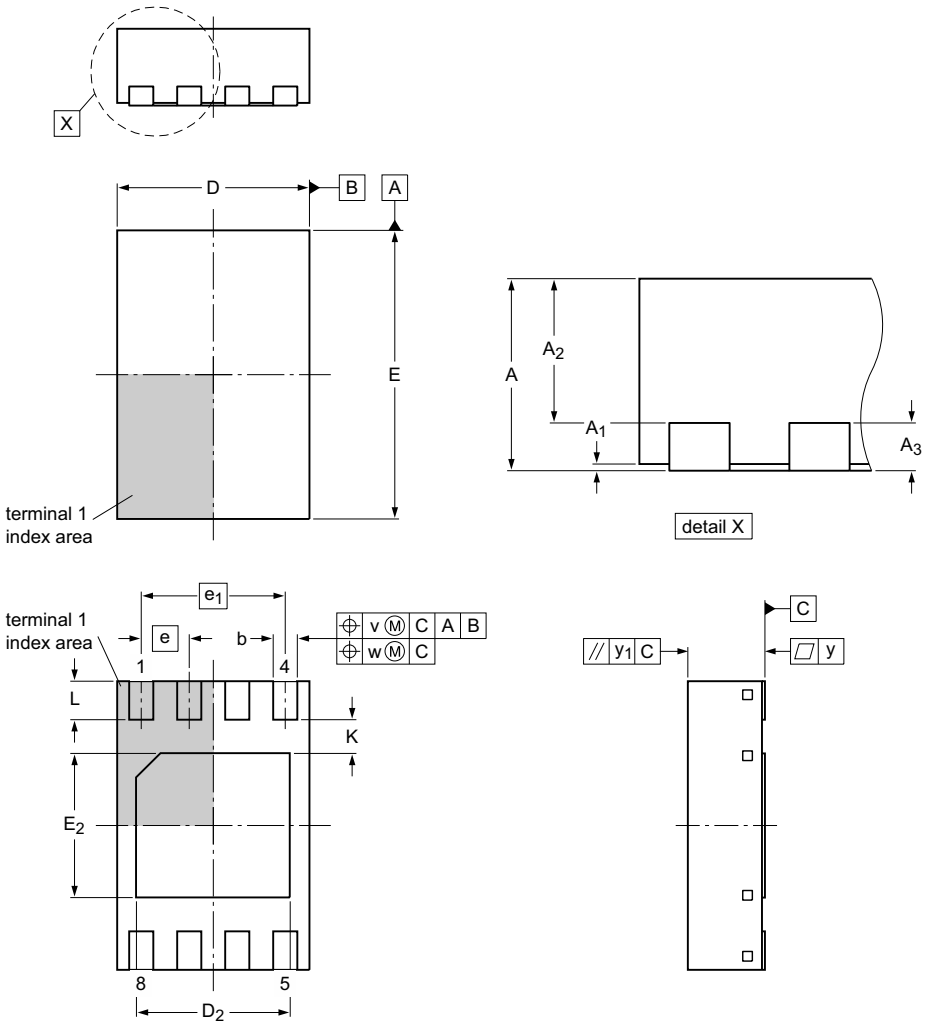
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 29. Package outline SOT505-1 (TSSOP8)

HWSON8: plastic thermal enhanced very very thin small outline package; no leads; 8 terminals; body 2 x 3 x 0.75 mm **SOT1069-2**



Dimensions

Unit		$A^{(1)}$	A_1	A_2	A_3	b	$D^{(1)}$	D_2	$E^{(1)}$	E_2	e	e_1	K	L	v	w	y	y_1
	max	0.80	0.05	0.65		0.30	2.1	1.6	3.1	1.6			0.40	0.45				
mm	nom	0.75	0.02	0.55	0.2	0.25	2.0	1.5	3.0	1.5	0.5	1.5	0.35	0.40	0.1	0.05	0.05	0.05
	min	0.70	0.00	0.45		0.18	1.9	1.4	2.9	1.4			0.30	0.35				

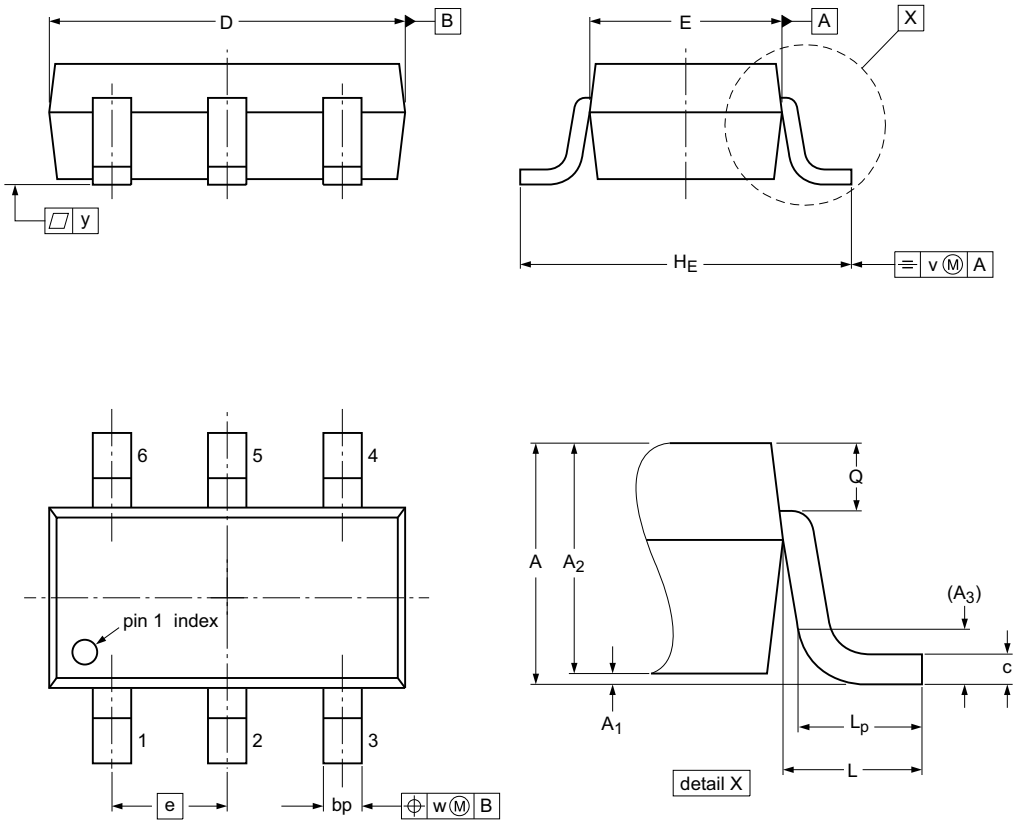
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1069-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1069-2	- - -	MO-229	- - -			~~09-11-18~~ 12-04-18

Fig 30. Package outline SOT1069-2 (HWSON8)

TSOP6: Plastic thin small outline package; 6 leads **SOT1353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D	E	e	H_E	L	L_p	Q	v	w	y
mm	max	1.1	0.1	1.0		0.40	0.26	3.1	1.7		3.0		0.6	0.33			
	nom				0.23					0.95		0.58			0.2	0.2	0.1
	min	0.9	0.013	0.9		0.25	0.10	2.7	1.3		2.5		0.2	0.23			

sot1353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1353-1	- - -	- - -	SC-74			~~13-03-20~~ 13-04-18

Fig 31. Package outline SOT1353-1 (TSOP6)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 32) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 22 and 23

Table 22. SnPb eutectic process (from J-STD-020D)

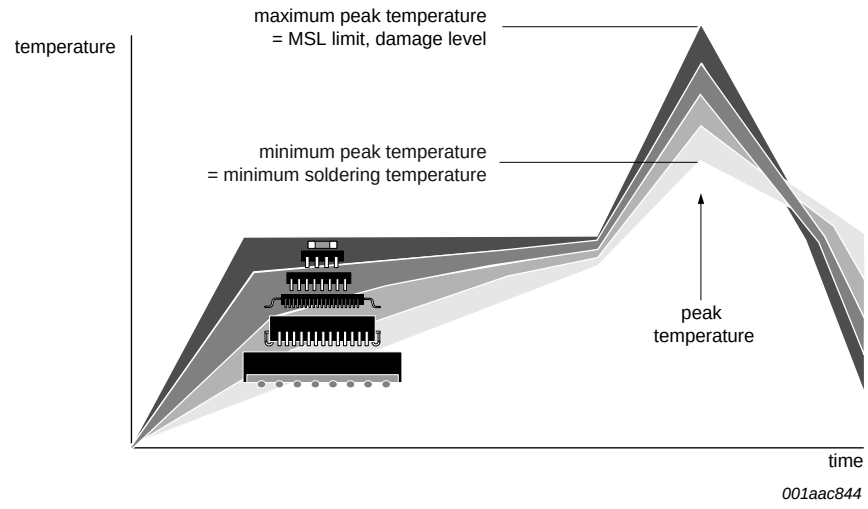
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 23. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 32.



MSL: Moisture Sensitivity Level

Fig 32. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Soldering: PCB footprints

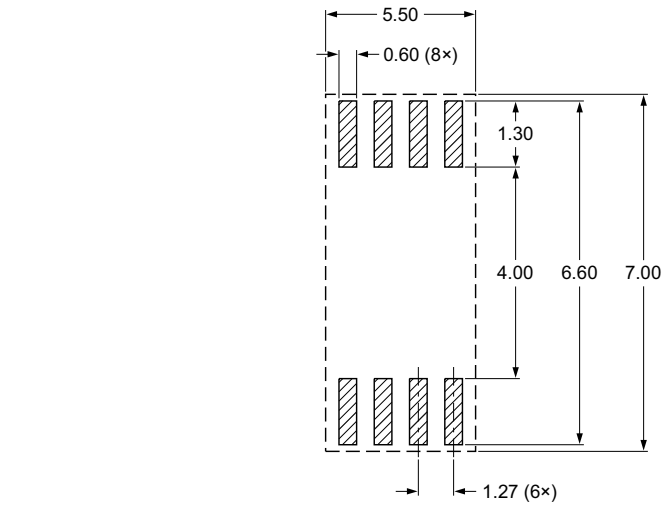


Fig 33. SOT96-1 (SO8); reflow soldering

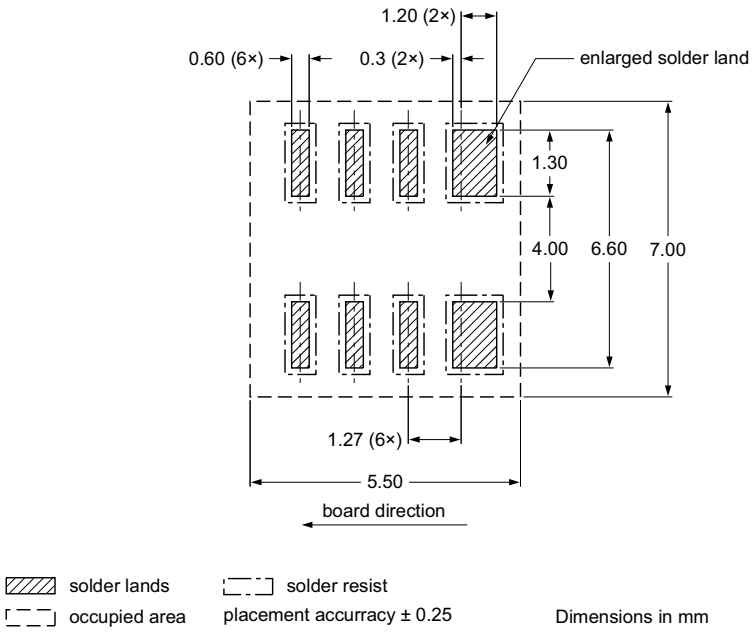


Fig 34. SOT96-1 (SO8); wave soldering

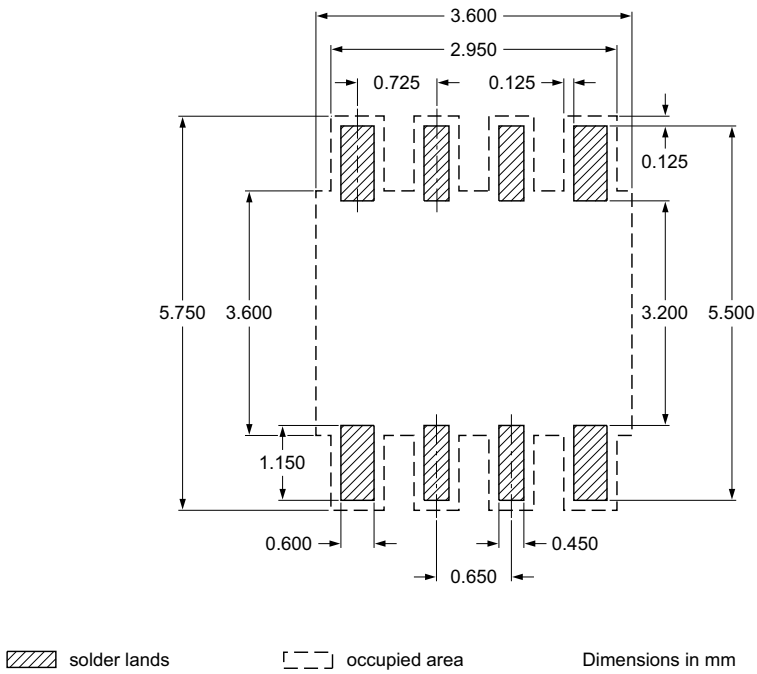
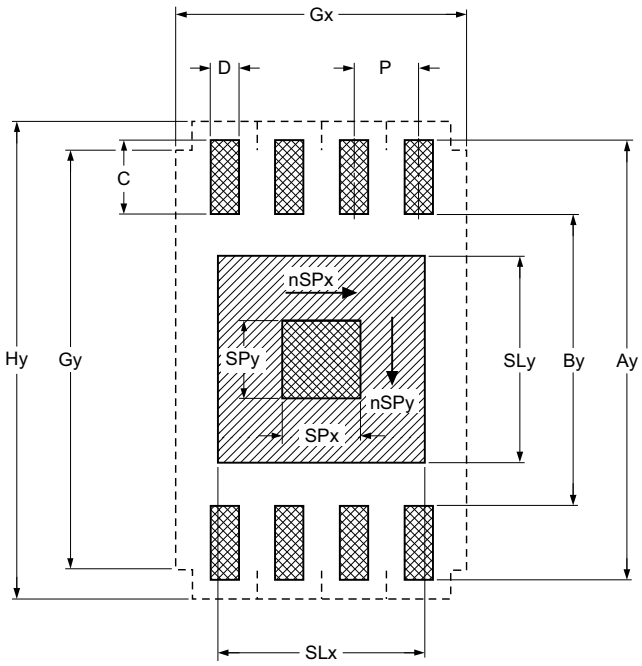


Fig 35. SOT505-1 (TSSOP8); reflow soldering

Footprint information for reflow soldering of HWSON8 package SOT1069-2



solder land

solder paste deposit

solder land plus solder paste

occupied area

DIMENSIONS in mm

P	Ay	By	C	D	SLx	SLy	SPx	SPy	Gx	Gy	Hy	nSPx	nSPy
0.5	3.45	2.2	0.625	0.25	1.6	1.6	0.6	0.6	2.25	3.25	3.7	1	1

Issue date ~~12-02-09~~ 12-02-22 sot1069-2_fr

Fig 36. SOT1069-2 (HWSON8); reflow soldering

16. Abbreviations

Table 24. Abbreviations

Acronym	Description
A-to-D	Analog-to-Digital
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LSB	Least Significant Bit
LSByte	Least Significant Byte
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed-Circuit Board
POR	Power-On Reset
SMD	Solder Mask Defined

17. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCT2075 v.10	20171120	Product data sheet	-	PCT2075 v.9.1
Modifications:	• Removed “X” in part number PCT2075GV/N005X • Section 4 “Ordering information”: Added PCT2075GV/P110 • Table 7 “Register table”: Added register information for PCT2075GV/P110			
PCT2075 v.9.1	20170421	Product data sheet	-	PCT2075 v.9
Modifications:	• Section 4 “Ordering information”: Added PCT2075GV/N005X • Table 7 “Register table”: Added register information for PCT2075GV/N005X • Added Figure 1 “Cooling system using custom part PCT2075GV/N005”			
PCT2075 v.9	20141024	Product data sheet	-	PCT2075 v.8
Modifications:	• Table 1 “Ordering information”: Changed topside mark of PCT2075GV from ‘075’ to ‘20x’; added Table note [1] • Table 2 “Ordering options”: Added PCT2075GVX			
PCT2075 v.8	20140925	Product data sheet	-	PCT2075 v.7
PCT2075 v.7	20140306	Product data sheet	-	PCT2075 v.6
PCT2075 v.6	20140124	Product data sheet	-	PCT2075 v.5
PCT2075 v.5	20131209	Product data sheet	-	PCT2075 v.4
PCT2075 v.4	20130719	Product data sheet	-	PCT2075 v.3
PCT2075 v.3	20130521	Product data sheet	-	PCT2075 v.2
PCT2075 v.2	20130506	Product data sheet	-	PCT2075 v.1
PCT2075 v.1	20130405	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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