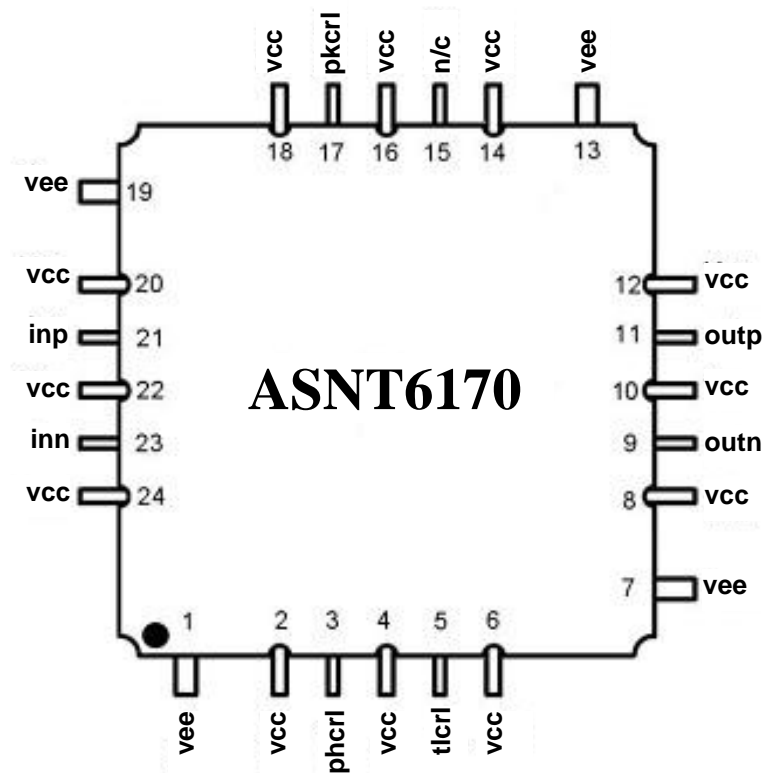# ASNT6170-KMC
DC-20*GHz* Analog Signal Adjustable Delay

- Broadband (DC-20*GHz*) tunable analog signal delay

- Utilizes discrete and continuous phase adjustment mechanisms

- Combined delay adjustment range of 12*ps*

- Utilizes internal peaking control for bandwidth adjustment

- Fully differential CML-type input interface

- Fully differential CML-type output interface

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 560*mW*

- Fabricated in SiGe for high performance, yield, and reliability
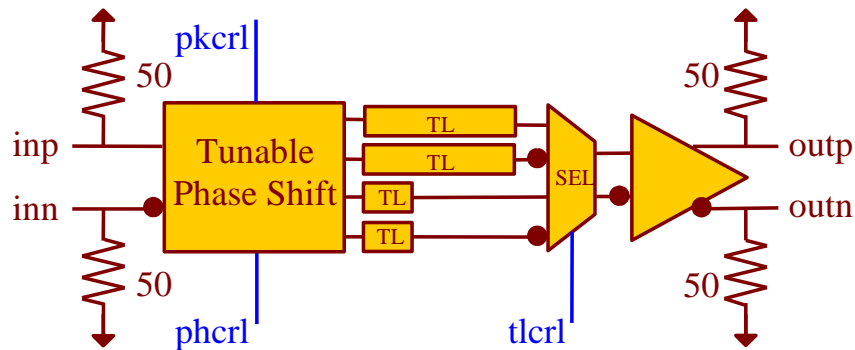
- Custom CQFP 24-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram (Negative Power Supply Mode)

ASNT6170-KMC is a variable delay line for analog signals fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal inp/inn. The delay is controlled through a DC control switch tlcrl and a DC tuning port phcrl for fine adjustment. The DC tuning port pkcrl may be used to increase the part's bandwidth at the cost of its delay range. The ports phcrl and pkcrl should be always connected to external voltage sources!

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

Delay Control Ports

The delay is controlled through a DC control switch tlcrl and a DC tuning port phcrl. The delay control diagram at pkcrl=vcc-2*V* is shown in Fig. 2. All voltage values are relative to vcc.
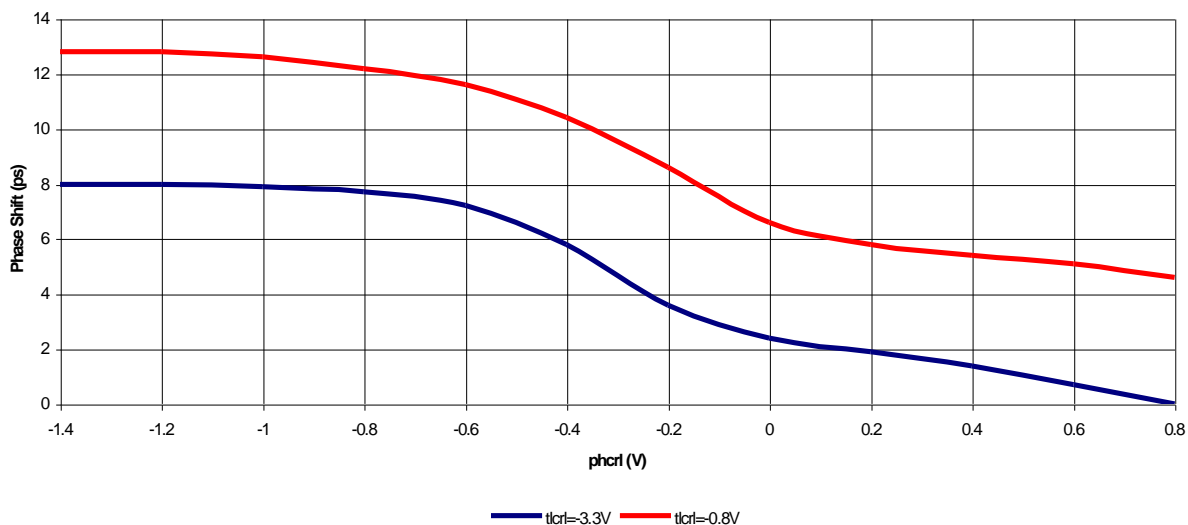

Fig. 2. Delay Control Diagram

Peak Control Port

The bandwidth (at *-3dB*) may be adjusted through a DC tuning tlcrl and a DC tuning port pkcrl. The bandwidth control diagram is shown in Fig. 3.
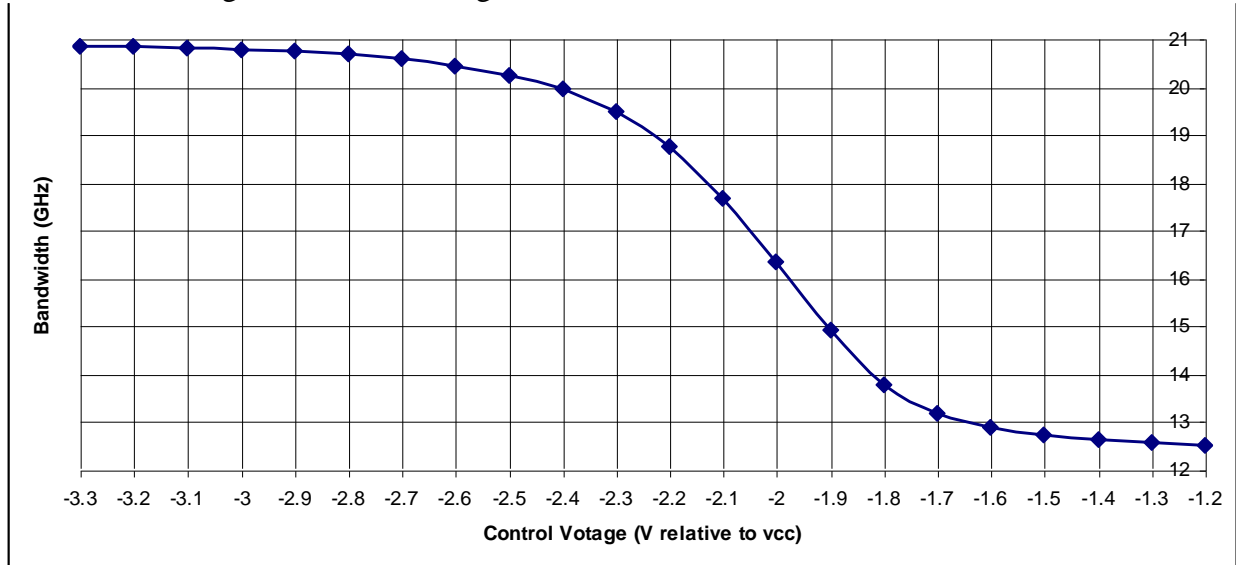

Fig. 3. Bandwidth vs. Control Voltage pkcrl

Linearity

Linearity of 6170 depends on the input signal's amplitude and frequency. Fig. 4 and Fig. 5 show worst-case simulated values of the second harmonic distortion (SHD) and the third harmonic distortion (THD) respectively on the input amplitude for 1*GHz*, 10*GHz*, and 15*GHz*. The graphs should be used for illustration purposes only. Preliminary test results demonstrate a better performance of SHD and THD less than *-50dBc* at 100*mV* input amplitude (200*mV* swing p-p) and 15*GHz* input frequency, as reflected in ELECTRICAL CHARACTERISTICS.
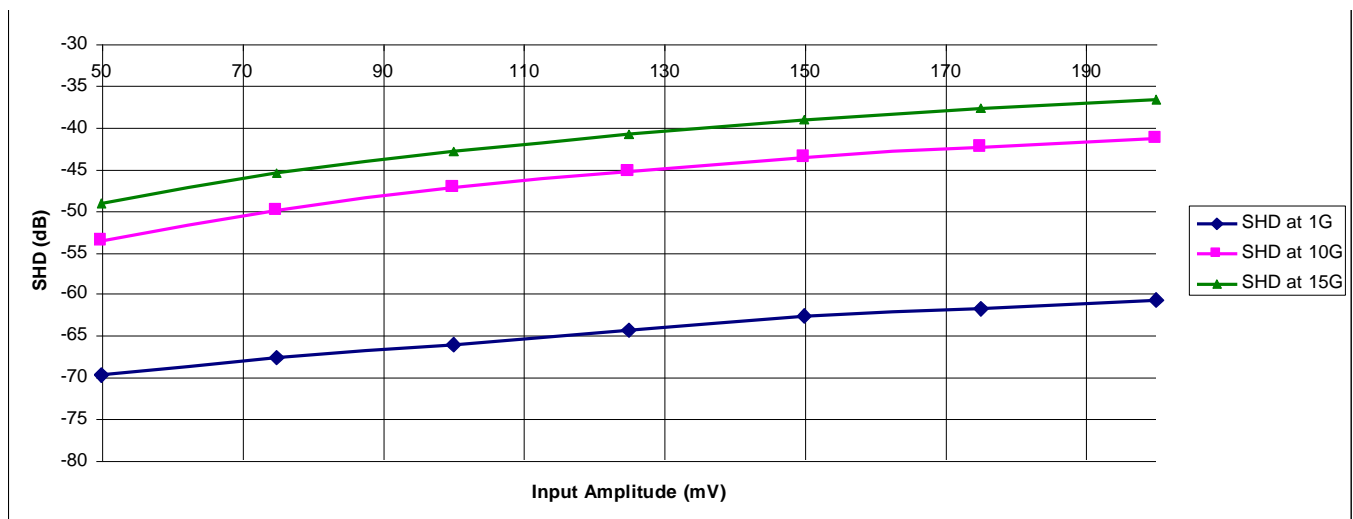

Fig. 4. Simulated SHD vs. Input Amplitude for 1 GHZ, 10 GHz , and 15 GHz Signals
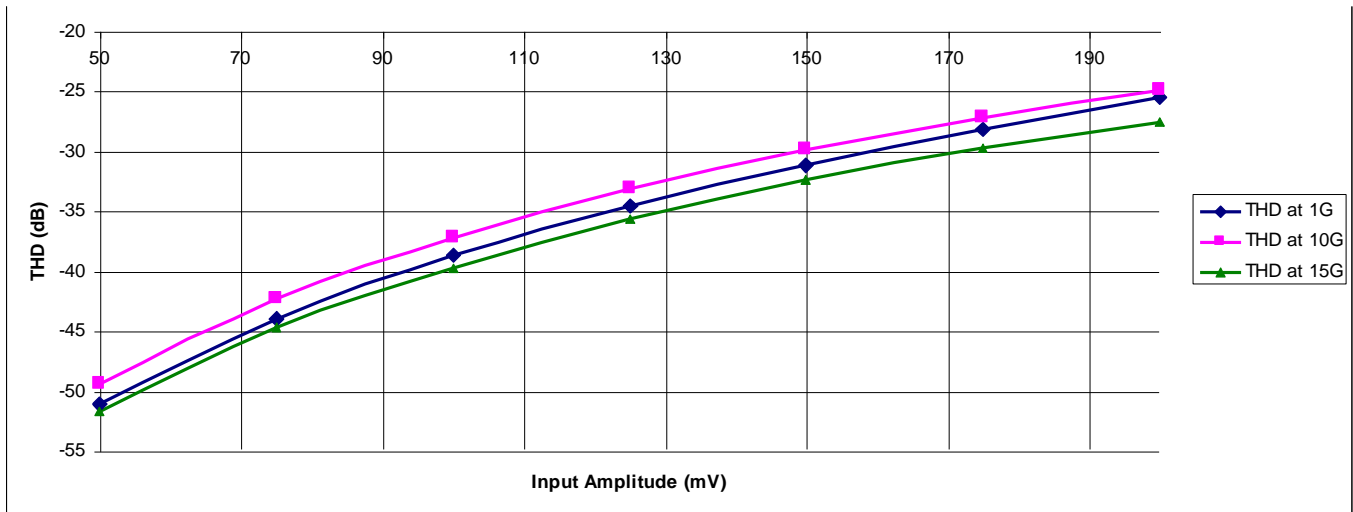
Fig. 5. Simulated THD vs. Input Amplitude for 1GHZ, 10GHz , and 15GHz Signals

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		620	*mW*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

Pin #	Pin name	Pin type	Pin function	Termination or connection
1	vee	supply voltage	negative power supply	GND
2	vcc	supply voltage	positive power supply	
3	phcrl	analog voltage	phase shift control	High impedance[1]
4	vcc	supply voltage	positive power supply	
5	tlcrl	CMOS input	additional delay on/off	$1MOhm$ to vee
6	vcc	supply voltage	positive power supply	
7	vee	supply voltage	negative power supply	GND
8	vcc	supply voltage	positive power supply	
9	outn	analog output	HS output data, inverted	$50Ohm$ to vcc
10	vcc	supply voltage	positive power supply	
11	outp	analog output	HS output data, direct	$50Ohm$ to vcc
12	vcc	supply voltage	positive power supply	
13	vee	supply voltage	negative power supply	GND
14	vcc	supply voltage	positive power supply	
15	n/c		not used	
16	vcc	supply voltage	positive power supply	
17	pkcrl	analog voltage	bandwidth control	High impedance[1]
18	vcc	supply voltage	positive power supply	
19	vee	supply voltage	negative power supply	GND
20	vcc	supply voltage	positive power supply	
21	inp	analog input	HS input data, direct	$50Ohm$ to vcc
22	vcc	supply voltage	positive power supply	
23	inn	analog input	HS input data, inverted	$50Ohm$ to vcc
24	vcc	supply voltage	positive power supply	

1) – This port should be always connected to an external voltage source

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		170		*mA*	
Power consumption		560		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input (inp/inn)					
Frequency	DC		20	*GHz*	
Swing	0.025		0.5	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output (outp/outn)					
Frequency	DC		20	*GHz*	
Gain		0		*dB*	Differential input to differential output
Harmonic distortions		-50		*dBc*	2nd and 3rd harmonics at $15GHz/200mVp\text{-}p$
DC Input Switch Control (tlcrl)					
Logic "1" level		vee+2.5		*V*	Switches between short and long
Logic "0" level		vee		*V*	transmission line paths
Tuning port (phcrl)					
Voltage level	vcc-1.4		vcc+0.8	*V*	Analog control for continuous delay adjustment
Output-to-Input Delay					
Phase shift	0		12	*ps*	For the full range of phcrl and both positions of tlcrl control switch
Tuning port (pkcrl)					
Voltage level	vcc-3.3		vcc-1.3	*V*	Peak control for BW adjustment, vee=-3.3*V*

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 6. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6170-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.
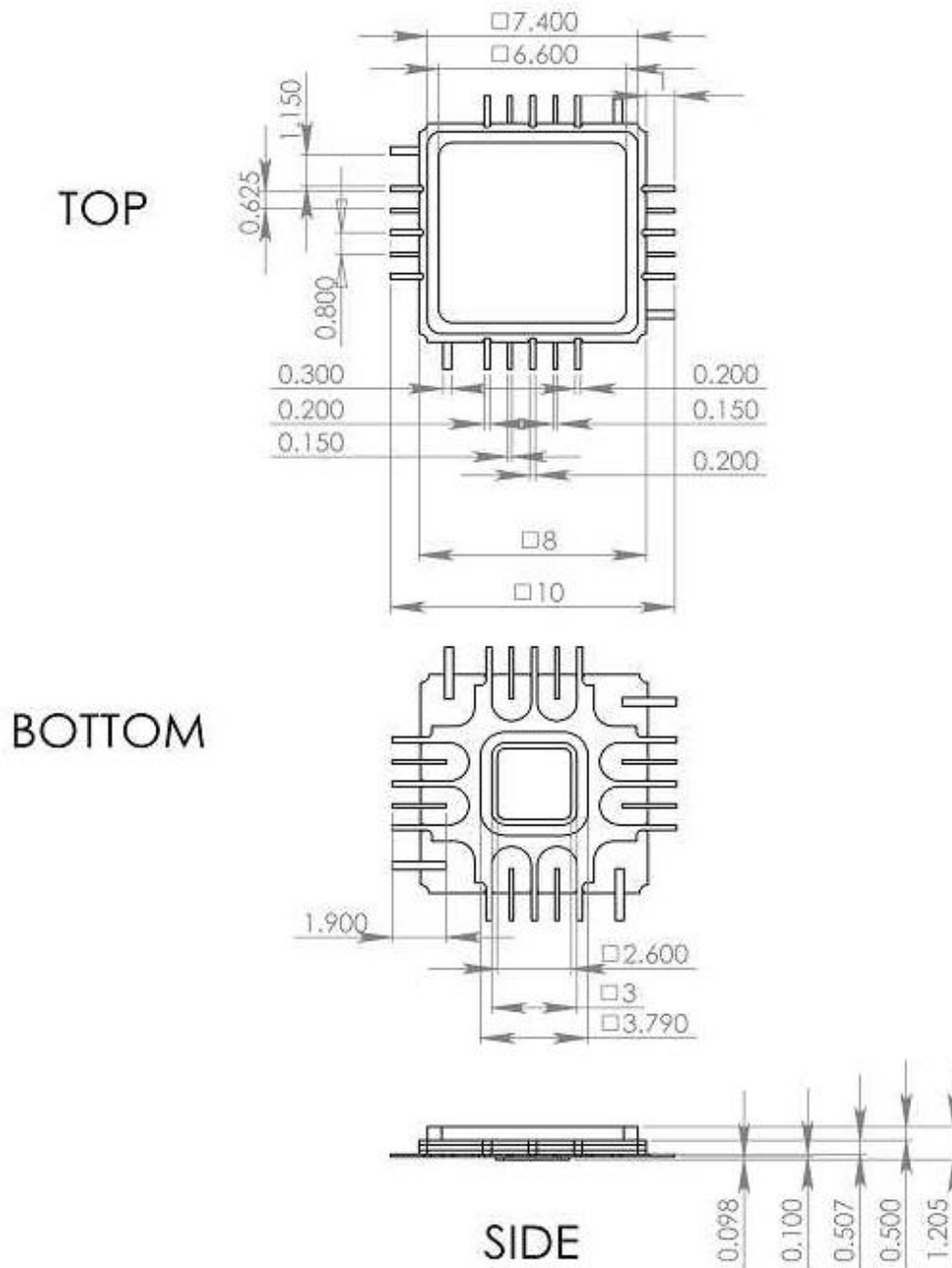
Fig. 6. CQFP 24-Pin Package Drawing (All Dimensions in mm)

REVISION HISTORY

Revision	Date	Changes
1.2.2	05-2020	Updated Package Information
1.1.2	07-2019	Updated Letterhead
1.1.1	02-2016	Corrected Peak Control Port section
1.0.1	05-2015	Initial release