

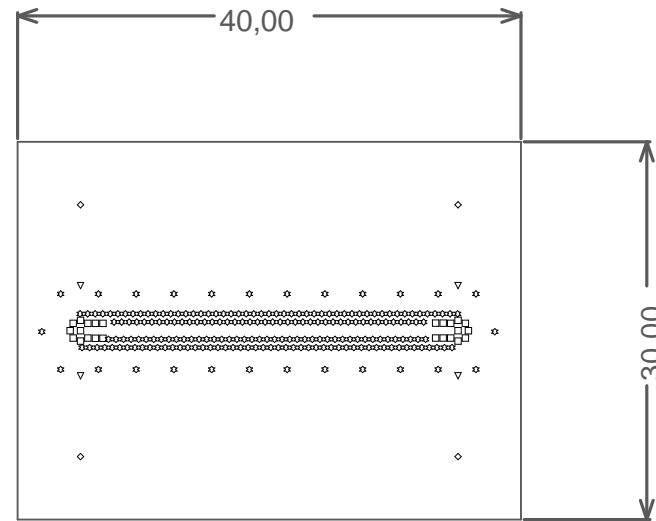
Beschreibung der Dokumente / Description of documents

|   |      |
|---|------|
| Top Layer                               | .GTL |
| Signal Layer 1                          | .G1  |
| Bottom Layer                            | .GBL |
| Top Solder Mask                         | .GTS |
| Bottom Solder Mask                      | .GBS |
| Board Outline                           | .GM5 |
| Via Filling Overplated / drill diameter | .GM9 |
| Bohrungen                               | .TXT |

| Symbol | Hit Count        | Hole Size           | Plated | Hole Type |
|--------|------------------|---------------------|--------|-----------|
| □      | 24               | 0,200mm (7,87mil)   | PTH    | Round     |
| ✳      | 212              | 0,300mm (11,81mil)  | PTH    | Round     |
| ▽      | 4                | 1,600mm (62,99mil)  | PTH    | Round     |
| ◇      | 4                | 3,300mm (129,92mil) | PTH    | Round     |
|        | <b>244 Total</b> |                     |        |           |

Für Signalvias gilt: Angabe ist Bohrdurchmesser / For signalvias: Hole size is drill diameter

Siehe mechanischer Layer 9 / see mechanical layer 9



Leiterplattengröße / PCB size 40,00 x 30,00 mm

|   |     |
|---|-----|
| Anzahl der Vias / Via count                     | 212 |
| Anzahl der Bohrungen / Hole count               | 244 |
| Anzahl der Langlöcher / Slot hole count         | 0   |
| Kontur gefräst / Board cutout with milling Tool |     |

Impedanzkontrollierte Leitungen / Controlled impedance:

Bottom Layer 50 Ohms referenced to Signal Layer 1 and GND on Bottom Layer Trace width 0,40mm, Gap 0,14mm

Alle Bohrungen mit Durchmesser 0,2mm sollen mit Via Filling Typ VII verschlossen werden. / All holes with diameter 0,2mm should be plugged with Via Filling Type VII.

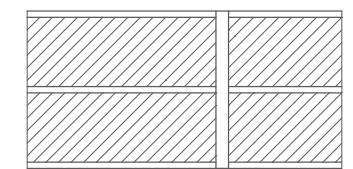
mechanischer Layer 9 kennzeichnet Via Filling und Bohrungen welche mit dem Bohrdurchmesser angegeben sind. / mechanical layer 9 marks Via Filling and vias which define drill diameter

Änderungshistorie / Document change record

| Rev. | change-no | affected   |           | Änderung / Summary of changes |
|------|-----------|------------|-----------|-------------------------------|
|      |           | PCB-Layout | Schematic |                               |
| 100  | 17-m003   | x          | x         | Neuanlage PCB / new PCB       |
|      |           |            |           |                               |
|      |           |            |           |                               |

Gesamtstärke / PCB thickness 0,9mm +/-10%

Alle Vias von Top nach Bottom. / all vias Top to Bottom.



Anzahl der Layer / Number of Layers 3

Die Kupferstärke auf den Außenlagen ist die Enddicke. Thickness of the outer Copper Layer are final.

| Layer | Name           | Material      | Thickness | Constant | Board Layer Stack |
|-------|----------------|---------------|-----------|----------|-------------------|
| 1     | Top Overlay    |               |           |          |                   |
| 2     | Top Solder     | Solder Resist | 0,010mm   | 3,5      |                   |
| 3     | Top Layer      | Copper        | 0,042mm   |          |                   |
| 4     | Dielectric1    | FR-4          | 0,500mm   | 4,4      |                   |
| 5     | Mid-Layer 1    | Copper        | 0,018mm   |          |                   |
| 6     | Dielectric2    | RO4350        | 0,254mm   | 3,48     |                   |
| 7     | Bottom Layer   | Copper        | 0,042mm   |          |                   |
| 8     | Bottom Solder  | Solder Resist | 0,010mm   | 3,5      |                   |
| 9     | Bottom Overlay |               |           |          |                   |

Fertigung der Leiterplatte entsprechend IPC-A-600 Class 2 in der aktuellen Auflage, sofern die Toleranzen unten nicht anders definiert sind. Fabrication according to IPC-A-600 class 2, current version, if below no other specification defined.

Leiterplatte ROHS-Konform, für bleifreien Reflow-Lötprozess geeignet (max. 260°C) und für Handlötung mit 325°C für 2s.

PCB ROHS-compliant, for leadfree reflow-soldering process (max. 260°C) and for manual soldering with 325°C at 2s.

| Allgemeintoleranzen für Leiterplatten / General Tolerances PCB      |                                      |   |           |
|---|--------------------------------------|---|-----------|
| Kontur / Board outline  | +/-0,1mm                             | Leiterbreite / Conductive width   | +/-0,03mm |
| Lochbild / Hole pattern   | +/-0,1mm                             | Stopplack zu Leiterbild / Solder resist mask to conductive pattern        | +/-0,1mm  |
| Lochbild zu Kontur / Hole pattern to board outline                  | +/-0,1mm                             | Beschriftung zu Leiterbild / Marking to conductive pattern                | +/-0,2mm  |
| Löcher / Holes  | +/-0,08mm                            | Lötdeckdruck zu Leiterbild / Peelable solder resist to conductive pattern | +/-0,2mm  |
| Leiterbild zu Lochbild / Conductive pattern to hole pattern         | +/-0,1mm                             | Kupfer auf Lochwandung / copper on hole wall                              | min. 20µm |
| Durchbrüche / Breakouts   | +/-0,1mm                             |   |           |
| Radien und Fasen / Radii and bevels                                 | +/-0,1mm                             |   |           |
| Leiterplattenoberfläche / PCB Surface                               |                                      |   |           |
| Freie Kupferoberfläche / Free copper                                | chem. Ni/Au (Ni 4-8µm, Au >= 0,05µm) |   |           |
| Lötstopplack fotosensitiv grün / Solder resist photosensitive green |                                      |   |           |

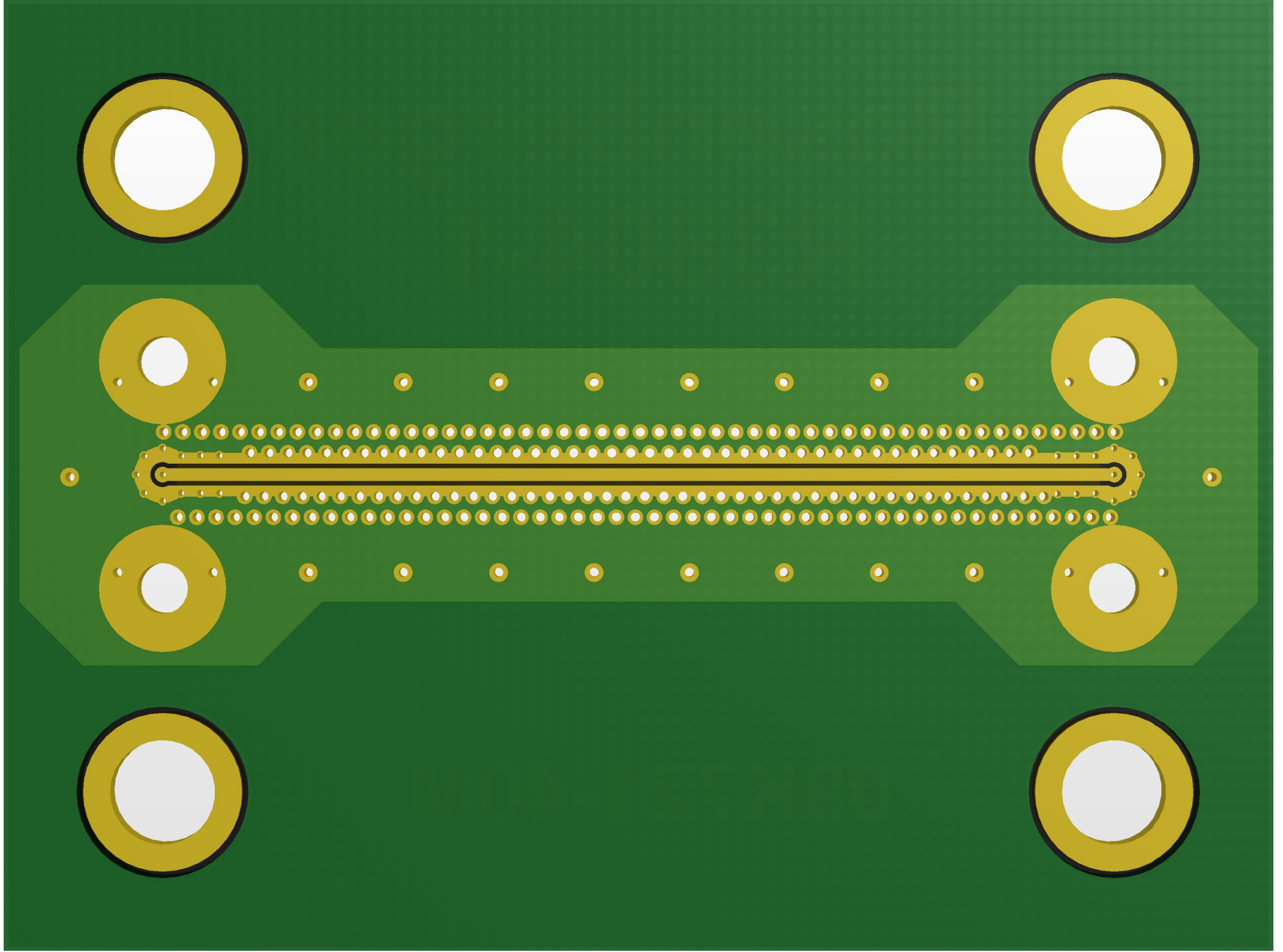
Nicht durchkontaktierte Bohrungen müssen frei von Kupfer und Verunreinigungen sein. / Non plated holes to be free of plating and contaminants.

| <b>Rosenberger</b><br>Hochfrequenztechnik GmbH & Co. KG |           |         |            | Project: 09K721-40M          |          |
|---|-----------|---------|------------|------------------------------|----------|
| vertraulich / confidential                              |           |         |            | Date                         | Name     |
|   |           |         |            | drawn 12.09.2017             | M_Krenn  |
|   |           |         |            | check. 26.09.2017            | H_Reiter |
|   |           |         |            | appr. 26.09.2017             | M_Moder  |
|   |           |         |            | Title: Testplatine           |          |
|   |           |         |            | drawing-no.: PCB-R3804-SU_DB |          |
|   |           |         |            | remarks:                     |          |
| 100   | 17-m003   | M_Krenn | 12.09.2017 |                              |          |
| Rev.  | change-no | Name    | Date       |                              |          |



**Rosenberger**  
**R3804-1**

**09K721-40M**





Darstellung 3-Lagen Aufbau mit Vias L1-L3

|   |                  |                               |               |
|---|------------------|-------------------------------|---------------|
| Research & Development<br><b>Rosenberger</b><br>Hochfrequenztechnik GmbH & Co. KG |                  | Title: Testplatine 09K721-40M |               |
| vertraulich / confidential  |                  | Variant: *                    | Revision: 100 |
| Developer: Marianne Krenn   | Date: 25.09.2017 | Time: 15:37:25                | Sheet: 1 of 1 |
| R3804.PrjPcb  | R3804.SchDoc     | SVN: Not in version control   |               |

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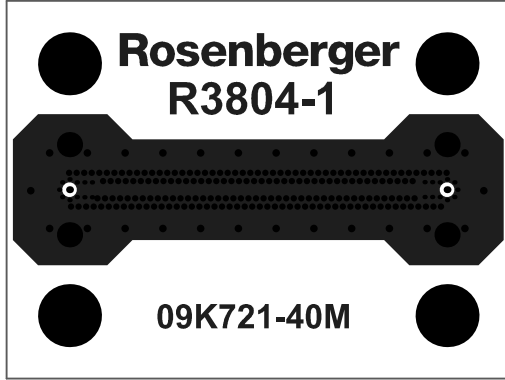
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| vertraulich / confidential |           |                   |            |
|                            |           | Date              | Name       |
|                            |           | drawn 12.09.2017  | M_Krenn    |
|                            |           | check. 26.09.2017 | H_Reiter   |
|                            |           | appr. 26.09.2017  | M_Moder    |
| 100                        | 17-m003   | M_Krenn           | 12.09.2017 |
| Rev.                       | change-no | Name              | Date       |

Project: 09K721-40M

Title: Testplatine

drawing-no.: PCB-R3804-SU\_DB

remarks:

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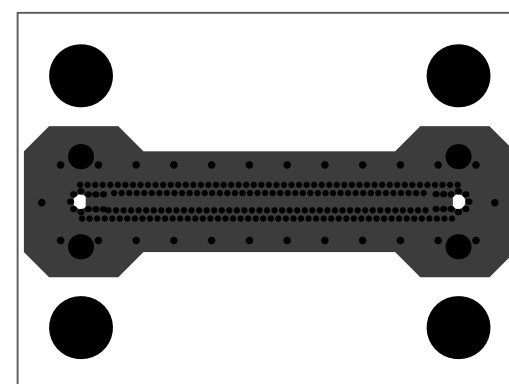
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|   |           |         |            | appr. 26.09.2017             | M_Moder  |
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| Rev.  | change-no | Name    | Date       | remarks:                     |          |

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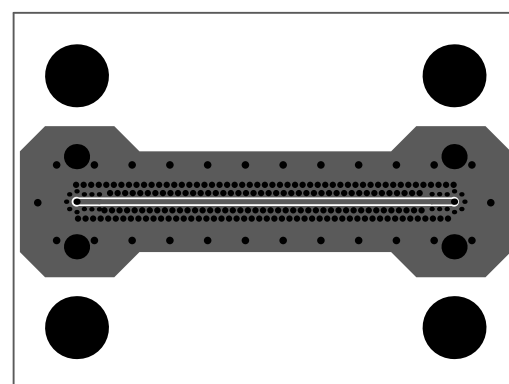
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| <b>Rosenberger</b>                |           |         |            | Project: |            | 09K721-40M   |                 |
| Hochfrequenztechnik GmbH & Co. KG |           |         |            | Title:   |            | Testplatine  |                 |
| vertraulich / confidential        |           |         |            | Date     | Name       | drawing-no.: |                 |
|                                   |           |         |            | drawn    | 12.09.2017 | M_Krenn      | PCB-R3804-SU_DB |
|                                   |           |         |            | check.   | 26.09.2017 | H_Reiter     |                 |
|                                   |           |         |            | appr.    | 26.09.2017 | M_Moder      |                 |
| 100                               | 17-m003   | M_Krenn | 12.09.2017 | remarks: |            |              |                 |
| Rev.                              | change-no | Name    | Date       |          |            |              |                 |

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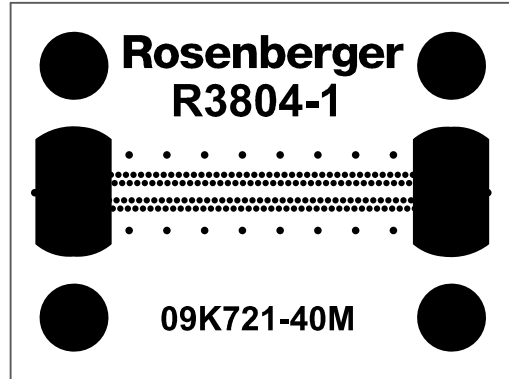
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| Rev.                       | change-no | Name              | Date       |

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Title: Testplatine

drawing-no.: PCB-R3804-SU\_DB

remarks:

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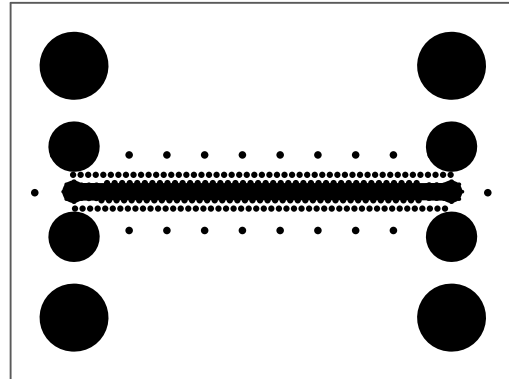
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| <b>Rosenberger</b>                |           |         |            |        |            | Project:        |             |
| Hochfrequenztechnik GmbH & Co. KG |           |         |            |        |            | 09K721-40M      |             |
| vertraulich / confidential        |           |         |            | Date   | Name       | Title:          |             |
|                                   |           |         |            | drawn  | 12.09.2017 | M_Krenn         | Testplatine |
|                                   |           |         |            | check. | 26.09.2017 | H_Reiter        |             |
|                                   |           |         |            | appr.  | 26.09.2017 | M_Moder         |             |
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| Title:       | Testplatine     |
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|                            |           |         | Name       |
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| 100                        | 17-m003   | M_Krenn | 12.09.2017 |
| Rev.                       | change-no | Name    | Date       |

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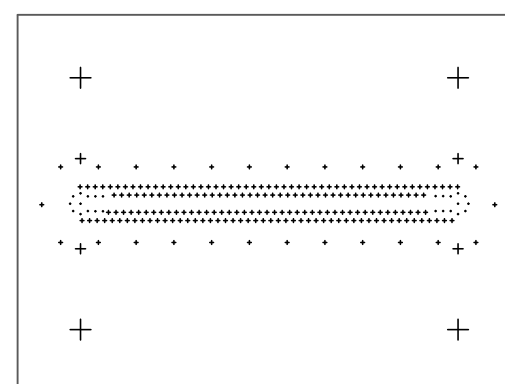
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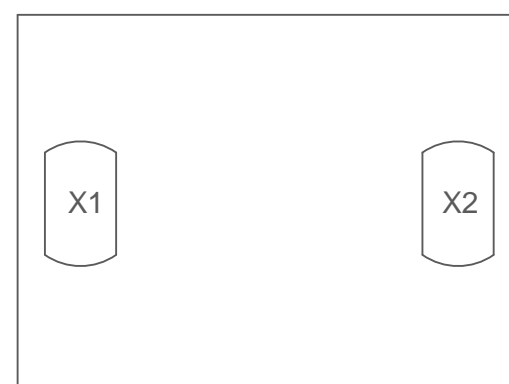
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