Qualcomm Technologies International, Ltd.

QTIL PCN 0104 Multiple Products

Product Change Notification

80-20343-1 Rev A

November 10, 2020

Product Change Notification

	QTILPCN Tracking #: 0104
Issue Date: 11/10/20	**Effective Date**: 11/10/20

Type of Change: A revision of the interface specification in the Data Sheets identified below.
Description of Change: Bitserial interface operating as a SPI Master (M-SPI) can operate at a maximum frequency of 8MHz (16MHz stated previously). The data-in setup time, T_{DIS}, has increased to 39ns (24.5ns stated previously).
Reason for Change: A review of on-chip static timing analysis determined that the on-chip delay between the Bitserial interface and device terminals is greater than previously stated.
Affected Product List: QCC-3020-0-CSP90-TR-00-0   QCC-3021-0-80PQFN-TR-00-0   QCC-3024-0-CSP90-TR-00-0   QCC-3026-0-81WLNSP-TR-00-0   QCC-3031-0-80PQFN-TR-00-0   QCC-3034-0-CSP90-TR-00-0   QCC-3040-0-CSP90B-TR-00-0   QCC-3044-0-CSP90B-TR-00-0   QCC-3046-0-WLNSP94B-TR-01-0   QCC-5120-0-124CSP-TR-00-0   QCC-5121-0-81WLNSP-TR-00-0   QCC-5124-0-CSP90-TR-00-0   QCC-5125-0-CSP90-TR-00-0   QCC-5126-0-CSP90-TR-01-0   QCC-5127-0-124CSP-TR-00-0   QCC-5141-0-WLNSP94B-TR-01-0   QCC-5144-0-CSP90B-TR-01-0
Data to Justify Change: Revised static timing analysis measured the on-chip delay from the device terminals to be up to 39ns and is such that the previously stated maximum of 16MHz mode of operation is likely to be unusable on some parts.
Suggested Implementation Plan: Verify if you have used 16MHz Bitserial M-SPI mode in the design. If 16MHz Bitserial M-SPI mode is used, QTIL recommends the developer to update their software to limit the maximum clock speed used to 8MHz.

(Form 76-32515-14, Rev B)

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QTIL intends to restrict the maximum frequency of the Bitserial interface operating as a SPI Master (M-SPI) to 8MHz in future ADK releases.
Impact on Form, Fit & Function: Bitserial interface maximum speed reduction – see description above. No other interfaces or functionality are affected.
Impact on Software: In a future release from QTIL, the Bitserial API will be restricted to prevent clock frequencies above 8MHz from being used. Configuring the interface in M-SPI mode for a 16MHz clock rate will then set the clock to 8MHz. Other clock rates will be unaffected.
Affected Product documentation: 80-CF192-1 QCC5120 VFBGA DATA SHEET 80-CF193-1 QCC5121 WLCSP DATA SHEET 80-CF194-1 QCC5124 WLCSP DATA SHEET 80-CG072-1 QCC5125 VFBGA DATA SHEET 80-CG726-1 QCC5126 VFBGA DATA SHEET 80-CG876-1 QCC5127 VFBGA DATA SHEET 80-CG231-1 QCC3020 VFBGA DATA SHEET 80-CF195-1 QCC3021 QFN DATA SHEET 80-CG232-1 QCC3024 VFBGA DATA SHEET 80-CF475-1 QCC3026 WLCSP DATA SHEET 80-CG233-1 QCC3031 QFN DATA SHEET 80-CG234-1 QCC3034 VFBGA DATA SHEET 80-CH103-1 QCC5141 WLCSP PRODUCTION INFORMATION DATA SHEET 80-CH353-1 QCC5144 VFBGA DATA SHEET 80-CH155-1 QCC3040 VFBGA DATA SHEET 80-CH247-1 QCC3044 VFBGA DATA SHEET 80-CH146-1 QCC3046 WLCSP DATA SHEET
New Parts will be Identified by: This specification change applies to all QCC51xx and QCC302x/3x/4x date codes. There is no change to device marking and the change will impact all date codes for parts used in systems employing 16MHz M-SPI.

For questions and information, please contact customer service at https://www.qualcomm.com/support