Sinusoidal 3-phase Brushless Motor Drivers with Sensorless Vector Control

SX68200M Series

Data Sheet

Description

The SX68200M series are 3-phase brushless motor drivers in which output transistors, pre-drive circuits, bootstrap diodes with current-limiting resistors are highly integrated. Employing a sinusoidal driving strategy with a sensorless vector control, the SX68200M series brings a small-sized, high-efficient, and low-noise motor controlling into your application.

These products can run on a 3-shunt current detection system and optimally control the inverter systems of medium-capacity motors that require universal input standards.

Features

- Pb-free (RoHS Compliant)
- UL-recognized: UL 60730-1 File No.:E99992 (SX68204M UL Recognition Pending)
- Sinusoidal Current Waveform (Low Noise, High Efficiency)
  Sensorless Vector Control (High Efficiency at Load Variation, Small Size)
- Built-in Bootstrap Diodes with Current-limiting Resistors
- EEPROM as a Control Parameter Storage
- Two Speed Control (PI Control) Modes:
  - Analog Voltage Control (VSP Pin)
  - Serial Communications Control (I^2C Compatible)
- 3-shunt Current Detection
- DIAG Pin Fault Signal Output
- Protections Include:
  - V3 Pin Undervoltage Protection
  - Watchdog Timeout Detection
  - Memory Error Detection
  - Overvoltage Protection and Undervoltage Lockout for Main Power Supply (VM Pin)
  - Soft Overcurrent Protection
  - Hard Overcurrent Protection
  - Thermal Warning
  - Thermal Shutdown
  - Undervoltage Lockout for Logic Supply
  - Loss-of-Synchronization Protection

Package

SOP36

Not to scale

Selection Guide

Part Number	V_{DSS}	I_O
SX68201M	250 V	2.0 A
SX68203M	600 V	1.5 A
SX68204M*	600 V	1.5 A
SX68205M	600 V	2.0 A

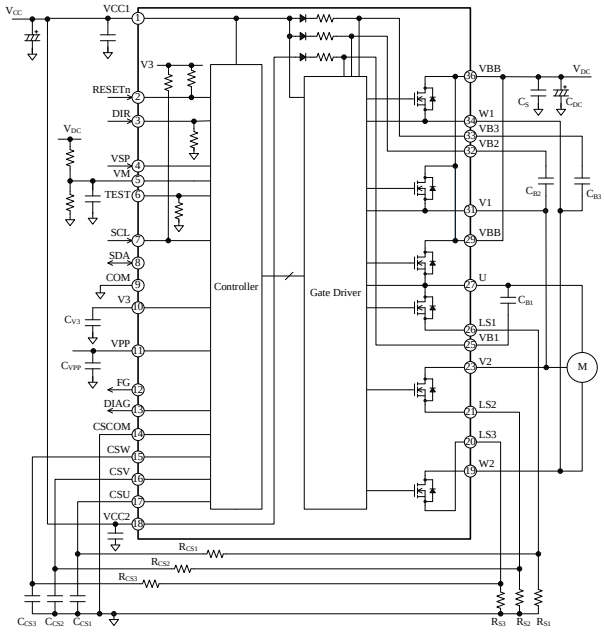
* Under development

Applications

For motor drives such as:

- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Typical Application



Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Power MOSFET Breakdown Voltage	V_{DSS}	V_{CC} = 15 V, I_D = 100 µA	250	V	SX68201M
			600		SX68203M SX68204M SX68205M
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	20	V	
	V_{BS}	VB1–U, VB2–V1, VB3–W1	20		
Output Current(1)	I_O	T_C = 25 °C, T_J < 150 °C	1.5	A	SX68203M SX68204M
			2.0		SX68201M SX68205M
Output Current (Pulse)	I_{OP}	T_C = 25 °C, V_{CC} = 15 V, pulse width ≤ 100 µs, duty cycle = 1%	2.25	A	SX68203M SX68204M
			3		SX68201M SX68205M
Logic Input Voltage	$V_{IN(1)}$	DIR–COM, SCL–COM, SDA–COM	−0.3 to 5.5	V	
	$V_{IN(2)}$	VSP–COM	−0.3 to 8.5	V	
Logic Output Voltage	V_O	FG–COM, DIAG–COM	−0.3 to V3 + 0.3	V	
VPP Pin Voltage	V_{PP}	VPP–COM	−0.3 to 28	V	
RESETn Pin Voltage	V_{RST}	RESETn–COM	−0.3 to 5.5	V	
VM Pin Voltage	V_{VM}	VM–COM	−0.3 to 4	V	
Input Pin Voltage for Current-sensing Operational Amplifier	V_{CSX}	CSU–COM, CSV–COM, CSW–COM, CSCOM–COM	−2 to 2	V	
Allowable Power Dissipation	P_D	T_A = 25 °C; when mounted on a board(2)	3.5	W	
Operating Case Temperature(3)	$T_{C(OP)}$		−25 to 100	°C	
Junction Temperature(4)	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Should be derated depending on an actual case temperature. See Section 14.2.
(2) Refers to a 1.6 mm thick CEM3 glass with 35 µm thick copper foil; measured under natural air-cooling without silicone potting.
(3) Refers to a case temperature measured during IC operation.
(4) Refers to the junction temperature of each chip built in the IC, including the control stage, gate drive stage, power MOSFETs, and bootstrap diodes.

2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–COM	—	140	200	V	SX68201M
			—	280	400		SX68203M SX68204M SX68205M
Logic Supply Voltage	V_{CC}	VCC1–COM, VCC2–COM	13.5	—	16.5	V	
	V_{BS}	VB1–U, VB2–V1, VB3–W1	13.5	—	16.5	V	
Input Voltage	$V_{IN(1)}$	DIR–COM, SCL–COM, SDA–COM	0	—	5.0	V	
	$V_{IN(2)}$	VSP–COM	0	—	5.88	V	
EEPRM Write Supply Voltage	V_{PP}		—	24	—	V	
Wait Time for Programming Supply Voltage Setup	t_{PRS}		50	—	—	ms	
VM Pin Input Voltage Range for Main Supply	V_M		0	—	1.8	V	
Dead Time of Input Signal	t_{DEAD}	DT[5:0] = [011110]	1.5	—	—	µs	
Bootstrap Capacitor	C_{BOOT}		1	—	10	µF	
Shunt Resistor*	R_{Sx}	$I_{OP} \leq 3.0$ A	0.22	—	—	Ω	SX68201M
		$I_{OP} \leq 2.25$ A	0.29	—	—		SX68203M SX68204M
		$I_{OP} \leq 3.0$ A	0.22	—	—		SX68205M

* Refers to the reference values calculated with a minimum value of V_{TRIPH}; should be a low-inductance resistor.

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V.

3.1. Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Operation						
VCCx Pin Logic Operation Start Voltage	$V_{CC(ON)}$	V_{CC} rising; VCC1–COM, VCC2–COM	10.5	11.5	12.5	V
VCCx Pin Logic Operation Stop Voltage	$V_{CC(OFF)}$	V_{CC} falling; VCC1–COM, VCC2–COM	10.0	11.0	12.0	V
VBx Pin Logic Operation Start Voltage	$V_{BS(ON)}$	V_{BS} rising; VB1–U, VB2–V1, VB3–W1	9.5	10.5	11.5	V
VBx Pin Logic Operation Stop Voltage	$V_{BS(OFF)}$	V_{BS} falling; VB1–U, VB2–V1, VB3–W1	9.0	10.0	11.0	V
VCCx Pin Logic Supply Current (in Operation)	I_{CC}	$V_{SP} > V_{SSX}$ with no oscillation; VCC1 = VCC2, VCC pin current in 3-phase operation	—	—	30	mA
VCCx Pin Logic Supply Current (in Low Power Consumption Mode)	I_{CCSTBY}	$V_{SP} < V_{VSSN}$	—	—	150	µA
VBx Pin Logic Supply Current	I_{BS}	V_{BS} = 15 V, V_{SP} = 5.4 V; VBx pin current in 1-phase operation	40	120	350	µA
Regulator Output Voltage	V_3	No load	3	3.3	3.7	V
Input Current for EEPROM Write Supply Voltage	I_{PP}		—	7	—	mA
VM Pin Input Voltage Range	V_M		0	—	1.8	V
VM Pin Input Current	I_{VM}	$0 < V_M < 1.8$ V	−2.5	—	2.5	µA
VSP Pin Input Current	I_{VSP}	V_{SP} = 5.5 V	10	—	45	µA
Input Signal						
DIR Pin Low Level Input Voltage[(1)]	V_{IL1}		—	—	0.76	V
DIR Pin High Level Input Voltage[(1)]	V_{IH1}		2.04	—	—	V
DIR Pin Internal Pull-down Resistor	R_{PD}		25	50	75	kΩ
RESETn Pin Low Level Input Voltage[(1)]	V_{ILR}		—	—	0.3	V
RESETn Pin High Level Input Voltage[(1)]	V_{IHR}		2.3	—	—	V
RESETn Pin Internal Pull-up Resistor	R_{PU}		—	90	—	kΩ
FG Pin High Level Output Voltage	V_{OH}	I_{OH} = −1 mA	V_3 − 0.5	V_3 − 0.2	V_3	V
DIAG Pin Internal Pull-up Resistor	R_{OH}		—	10	—	kΩ
DIAG Pin, FG Pin Low Level Output Voltage	V_{OL1}	I_{OH} = 1 mA	—	0.2	0.45	V

[(1)] When applying an external voltage, be sure to set the DIR and RESETn pins to logic low during IC startup (i.e., until the V3 pin voltage is established).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Motor Control						
VSP Pin Startup Voltage	V_{SSX}	V_{SP} rising	1.13	1.26	1.4	V
Hold Time for Initial Positioning(2)	t_{HOLD}		282	353	424	ms
Dead Time	DT		1.425	1.5	1.575	µs
Protection						
Current Limiting Value(2)	I_{LIM}		78	80	82	% I_{FS}
OCP Threshold Voltage(2)	V_{TRIPS}		0.39	0.40	0.41	V
VM Pin OVP Threshold Voltage(2)	V_{OVM}		1.1	1.24	1.35	V
VM Pin UVP Threshold Voltage(2)	V_{UVM}		0.20	0.29	0.38	V
V3 Pin UVP Threshold Voltage	V_{3UV}	V_3 falling	—	2.8	—	V
V3 Pin UVP Hysteresis	V_{3UVHYS}		—	175	—	mV
HOCP Threshold Current(2)	I_{HOCP}		130	150	165	% I_{FS}
HOCP Threshold Voltage(2)	V_{TRIPH}		650	750	825	mV
HOCP Filtering Time(2)	t_{HOCPF}		0.75	1.00	1.25	µs
TSD Temperature (Gate-drive MIC)	T_{DHD}		120	130	—	°C
TSD Hysteresis Temperature (Gate-drive MIC)	T_{DHYSD}		—	40	—	°C
Thermal Warning Temperature (Control MIC)	T_{WHC}		125	135	—	°C
Thermal Warning Temperature Hysteresis (Control MIC)	T_{WHYS}		—	15	—	°C
TSD Temperature (Control MIC)	T_{DHC}		135	150	—	°C
TSD Temperature Hysteresis (Control MIC)	T_{DHCHYS}		—	35	—	°C

(2) Reference value

3.2. Serial Communications

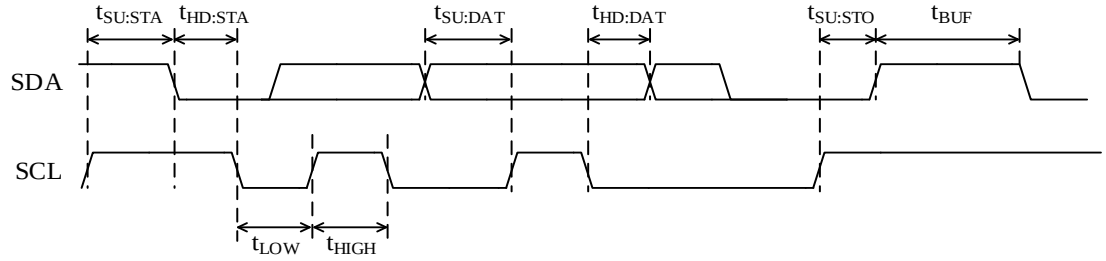


Figure 3-1. Serial Communications Timings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Glitch Suppression Filter(1)	—		—	—	50	ns
SCL Pin Clock Frequency	f_{CLK}		0	—	400	kHz
Falling Time of Output	t_{OF}	C = 400 pF, $V_{pull-up}$ = 3 V to 3.3 V	—	—	250	ns
Stop-to-Start Bus-free Time	t_{BUF}		1.3	—	—	µs
Start Condition Hold Time	$t_{HD:STA}$		0.6	—	—	µs
Start Condition Setting Time	$t_{SU:STA}$		0.6	—	—	µs
SCL Pin Low Level Time	t_{LOW}		1.3	—	—	µs
SCL Pin High Level Time	t_{HIGH}		0.6	—	—	µs
Data Setup Time	$t_{SU:DAT}$		100	—	—	ns
Data Hold Time	$t_{HD:DAT}$		0	—	900	ns
Stop Condition Setting Time	$t_{SU:STO}$		0.6	—	—	µs
SDA Pin Low Level Output Voltage	V_{OL}	I_{OL} = 3 mA	—	—	0.45	V
SDA Pin Output Leakage Current	I_O	V_O = 0 V to 5.5 V, V_3 = 0 V to 3.3 V	−2.5	—	2.5	µA
SDA or SCL Pin Low Level Input Voltage	V_{IL}		—	—	0.76	V
SDA or SCL Pin High Level Input Voltage (2)	V_{IH}		2.04	—	—	V
SCL Pin Input Pull-up Resistor(2)	R_{PU_S}		45	90	105	kΩ

(1) Refers to a pulse width for suppressing spike noise.
(2) When applying an external voltage, be sure to set the SDA and SCL pins to logic low during IC startup (i.e., until the V3 pin voltage is established).

3.3. Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections. V_{GS} represents the voltage between the gate and source of an internal power MOSFET.

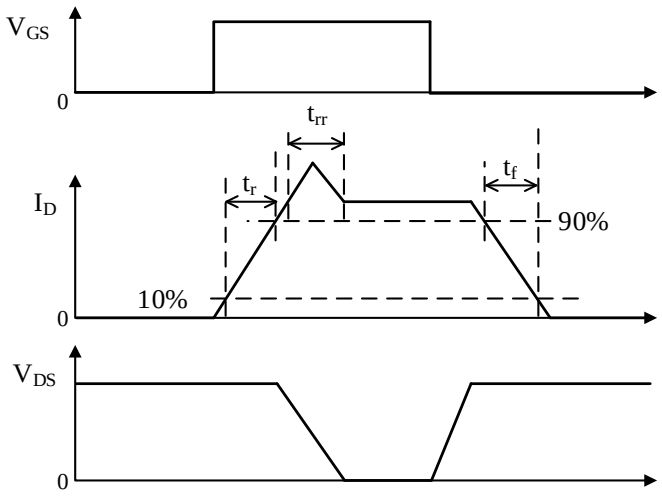


Figure 3-2. Switching Characteristics Definitions

3.3.1. SX68201M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 250 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1 A	—	1.25	1.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, T_J = 25 °C, inductive load	—	75	—	ns
Rise Time*	t_r		—	45	—	ns
Fall Time*	t_f		—	40	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, T_J = 25 °C, inductive load	—	70	—	ns
Rise Time*	t_r		—	50	—	ns
Fall Time*	t_f		—	20	—	ns

* Guaranteed by design.

3.3.2. SX68203M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.75 A	—	4.5	5.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75 A	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, T_J = 25 °C, inductive load	—	115	—	ns
Rise Time*	t_r		—	95	—	ns
Fall Time*	t_f		—	35	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, T_J = 25 °C, inductive load	—	110	—	ns
Rise Time*	t_r		—	95	—	ns
Fall Time*	t_f		—	35	—	ns

3.3.3. SX68204M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 0.75 A	—	2.9	3.6	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75 A	—	0.95	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, T_J = 25 °C, inductive load	—	125	—	ns
Rise Time*	t_r		—	60	—	ns
Fall Time*	t_f		—	25	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 0.75 A, T_J = 25 °C, inductive load	—	130	—	ns
Rise Time*	t_r		—	65	—	ns
Fall Time*	t_f		—	30	—	ns

* Guaranteed by design.

3.3.4. SX68205M

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1 A	—	2.0	2.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1 A	—	1.1	1.6	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.0 A, T_J = 25 °C, inductive load	—	115	—	ns
Rise Time*	t_r		—	50	—	ns
Fall Time*	t_f		—	45	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time*	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.0 A, T_J = 25 °C, inductive load	—	115	—	ns
Rise Time*	t_r		—	55	—	ns
Fall Time*	t_f		—	40	—	ns

3.4. Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.0	1.3	V
Bootstrap Diode Series Resistor	R_{BOOT}		45	60	75	Ω

3.5. Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case Thermal Resistance[1]	R_{J-C}	All power MOSFETs operating; when mounted on a board[2]	—	—	10	°C/W
Junction-to-Ambient Thermal Resistance	R_{J-A}		—	—	35	°C/W

[1] Refers to a case temperature at the measurement point described in Figure 3-3.
[2] Refers to a 1.6 mm thick CEM3 glass with 35 µm thick copper foil; measured under natural air cooling without silicone potting.

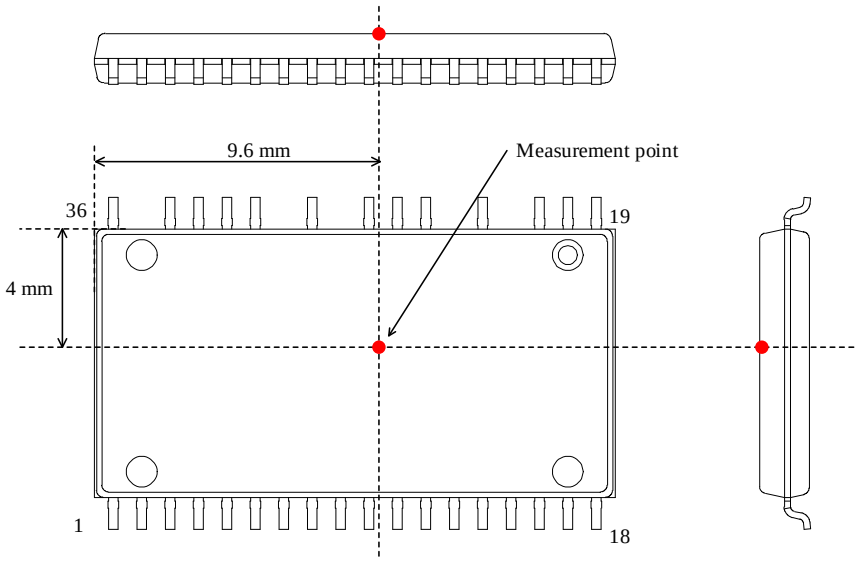


Figure 3-3. Case Temperature Measurement Point

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Package Weight		—	1.4	—	g

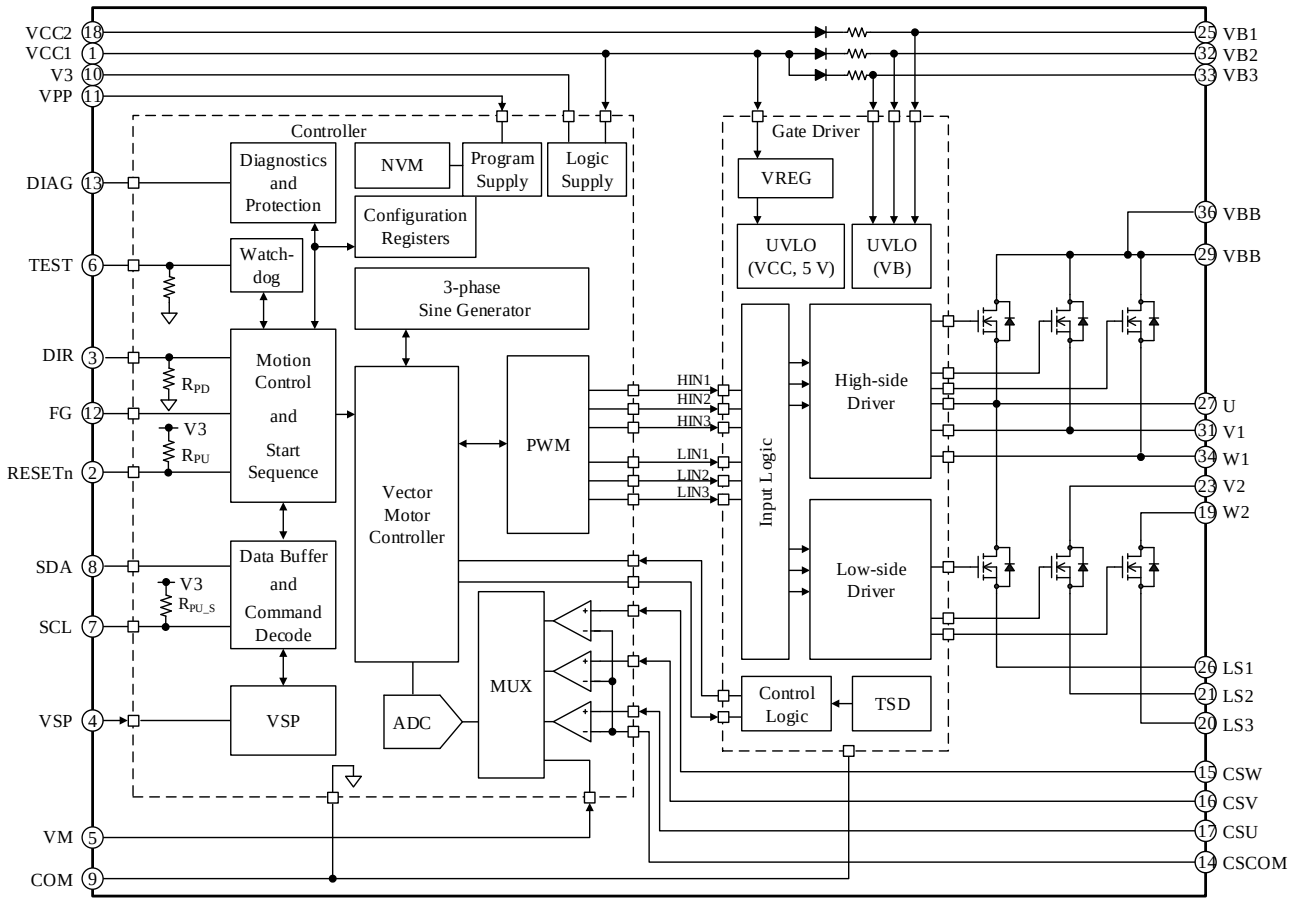
5. Reference Register Value

The table below lists the reference values to be written to the registers. All the values in parentheses are expressed in hexadecimal. The values listed in the table below are only the parameters that the GUI initially displays.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0							CR1	CR0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
Ref. Value (0047)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1
Config 1							DT5	DT4	DT3	DT2	DT1	DT0	OHT3	OHT2	OHT1	OHT0
Ref. Value (01E9)	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	1
Config 2							CMS1	CMS0	RSN1	RSN0	OCF1	OCF0	CD3	CD2	CD1	CD0
Ref. Value (0363)	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1	1
Config 3							MO3	MO2	MO1	MO0	BCG2	BCG1	BCG0	IWM1	IWM0	IHO
Ref. Value (0160)	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0
Config 4							HT5	HT4	HT3	HT2	HT1	HT0	HD3	HD2	HD1	HD0
Ref. Value (0054)	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0
Config 5							STS4	STS3	STS2	STS1	STS0	STD4	STD3	STD2	STD1	STD0
Ref. Value (0104)	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
Config 6							LS5	LS4	LS3	LS2	LS1	LS0	HS3	HS2	HS1	HS0
Ref. Value (0005)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
Config 7							IM4	IM3	IM2	IM1	IM0	IO4	IO3	IO2	IO0	IO0
Ref. Value (00D5)	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1
Config 8							UVS	HR3	HR2	HR1	HR0	FGS	SI3	SI2	SI1	SI0
Ref. Value (0106)	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0
Config 9								CP3	CP2	CP1	CP0	ETR	CI3	CI2	CI1	CI0
Ref. Value (00C6)	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0
Config 10								TP3	TP2	TP1	TP0		TI3	TI2	TI1	TI0
Ref. Value (00C6)	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0
Config 11							PWD9	PWD8	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
Ref. Value (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Config 12							LW9	LW8	LW7	LW6	LW5	LW4	LW3	LW2	LW1	LW0
Ref. Value (00C8)	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
Config 13							XWM1	XWM0	LHT1	LHT0	FW5	FW4	FW3	FW2	FW1	FW0
Ref. Value (000D)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
Config 14							DTC	VMC	DG3	DG2	DG1	DG0	DM3	DM2	DM1	DM0
Ref. Value (0100)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Config 15							SCS		PN3	PN2	PN1	PN0	SU3	SU2	SU1	SU0
Ref. Value (0209)	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1
Config 16							SR9 SRH9	SR8 SRH8	SR7 SRH7	SR6 SRH6	SR5 SRH5	SR4 SRH4	SR3 SRH3	SR2 SRH2	SR1 SRH1	SR0 SRH0
Ref. Value (001E)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
Config 17							SRL9	SRL8	SRL7	SRL6	SRL5	SRL4	SRL3	SRL2	SRL1	SRL0
Ref. Value (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

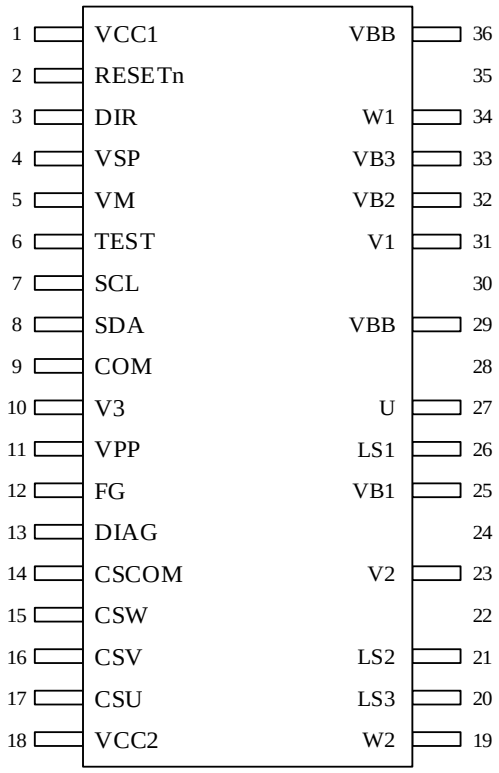
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 18							VX9	VX8	VX7	VX6	VX5	VX4	VX3	VX2	VX1	VX0
Ref. Value (0366)	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	0
Config 19							VS9	VS8	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
Ref. Value (01B3)	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
Config 20							VN9	VN8	VN7	VN6	VN5	VN4	VN3	VN2	VN10	VN0
Ref. Value (015C)	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0	0
Config 21							VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC11	VC0
Ref. Value (00AE)	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0
Register 28 Write EEPROM Control	0	0	0	0	0	0	SAV	0	0	0	0	0	0	0	0	0
Register 28 Read EEPROM Count	0	0	0	0	0	0	NVC9	NVC8	NVC7	NVC6	NVC5	NVC4	NVC3	NVC2	NVC1	NVC0
Register 29 Fault Mask							TW	OT	LOS	PMF	HOC	OVM	UVM			
Ref. Value (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Register 30 Write												DIAG4	DIAG3	DIAG2		
Ref. Value (0000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Register 30 Read Diagnostic	FF	POR	ME	WD	OC	EE	TW	OT	LOS	PMF	HOC	OVM	UVM	0	0	
Register 31 Run							DIAG1	DIAG0	RDG	PMR	STM	ESF	RSC	BRK	DIR	RUN
Ref. Value (0092)	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0
Register Read	FF	POR	ME	WD	OC	EE										

6. Block Diagram



7. Pin Configuration Definitions

Top View



Pin Number	Pin Name	Description
1	VCC1	Logic supply voltage input 1
2	RESETn	Reset signal input
3	DIR	Motor direction setting signal input
4	VSP	Motor speed control signal input
5	VM	Main supply voltage detection signal input
6	TEST	Test input
7	SCL	Serial clock input
8	SDA	Serial data input
9	COM	Logic ground
10	V3	Internal regulator (i.e., V3 regulator) output
11	VPP	EEPROM write supply voltage input
12	FG	Motor rotation pulse output
13	DIAG	Fault signal output
14	CSCOM	Current detection reference voltage input
15	CSW	W-phase current detection signal input
16	CSV	V-phase current detection signal input
17	CSU	U-phase current detection signal input
18	VCC2	Logic supply voltage input 2
19	W2	W-phase output (connected to W1 externally)
20	LS3	W-phase low-side power MOSFET source
21	LS2	V-phase low-side power MOSFET source
22	—	Pin removed
23	V2	V-phase output (connected to V1 externally)
24	—	Pin removed
25	VB1	U-phase high-side floating supply voltage input
26	LS1	U-phase low-side power MOSFET source
27	U	U-phase output
28	—	Pin removed
29	VBB	Positive DC bus supply voltage
30	—	Pin removed
31	V1	V-phase output (connected to V2 externally)
32	VB2	V-phase high-side floating supply voltage input
33	VB3	W-phase high-side floating supply voltage input
34	W1	W-phase output (connected to W2 externally)
35	—	Pin removed
36	VBB	Positive DC bus supply voltage

8. Typical Application

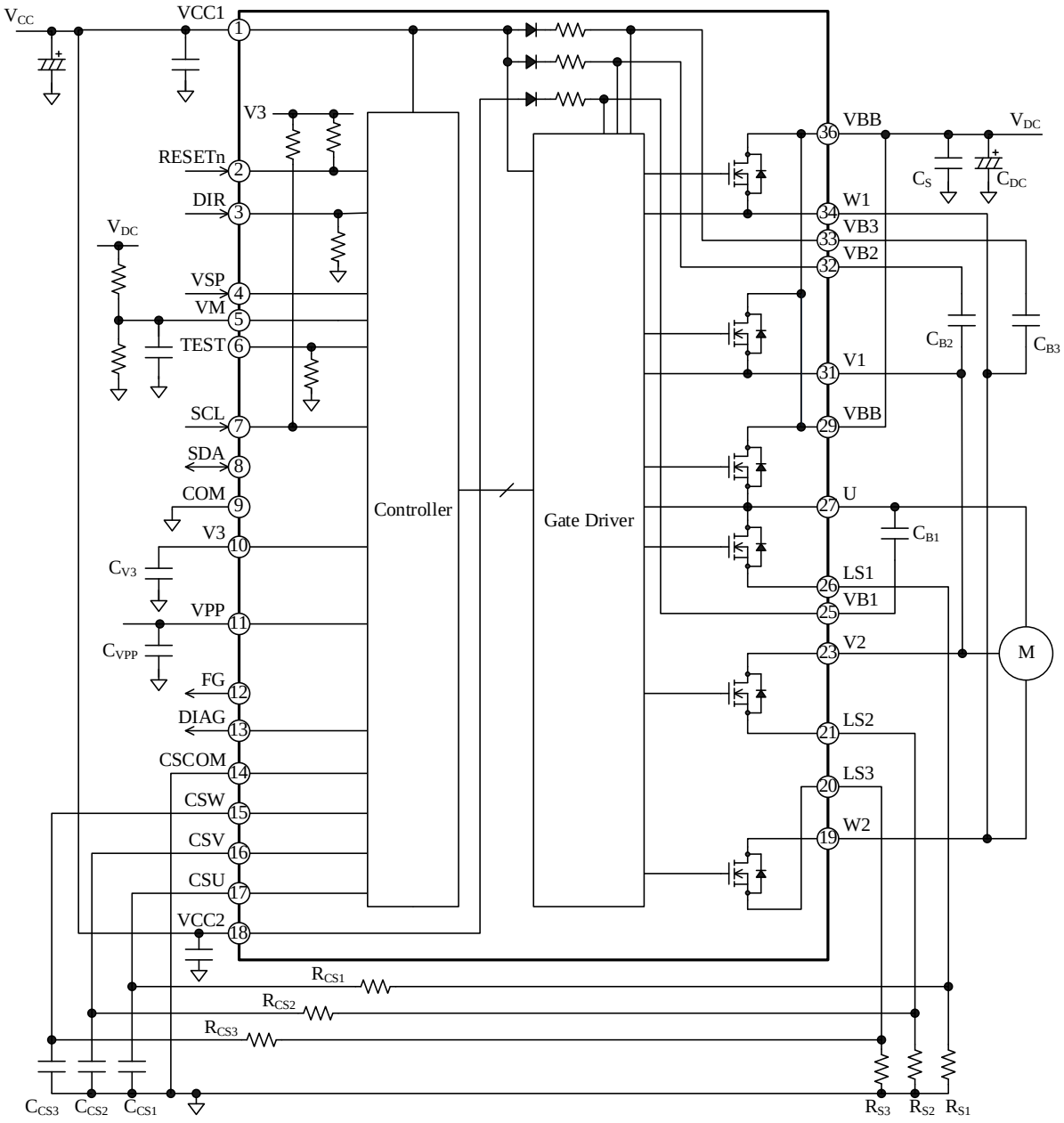
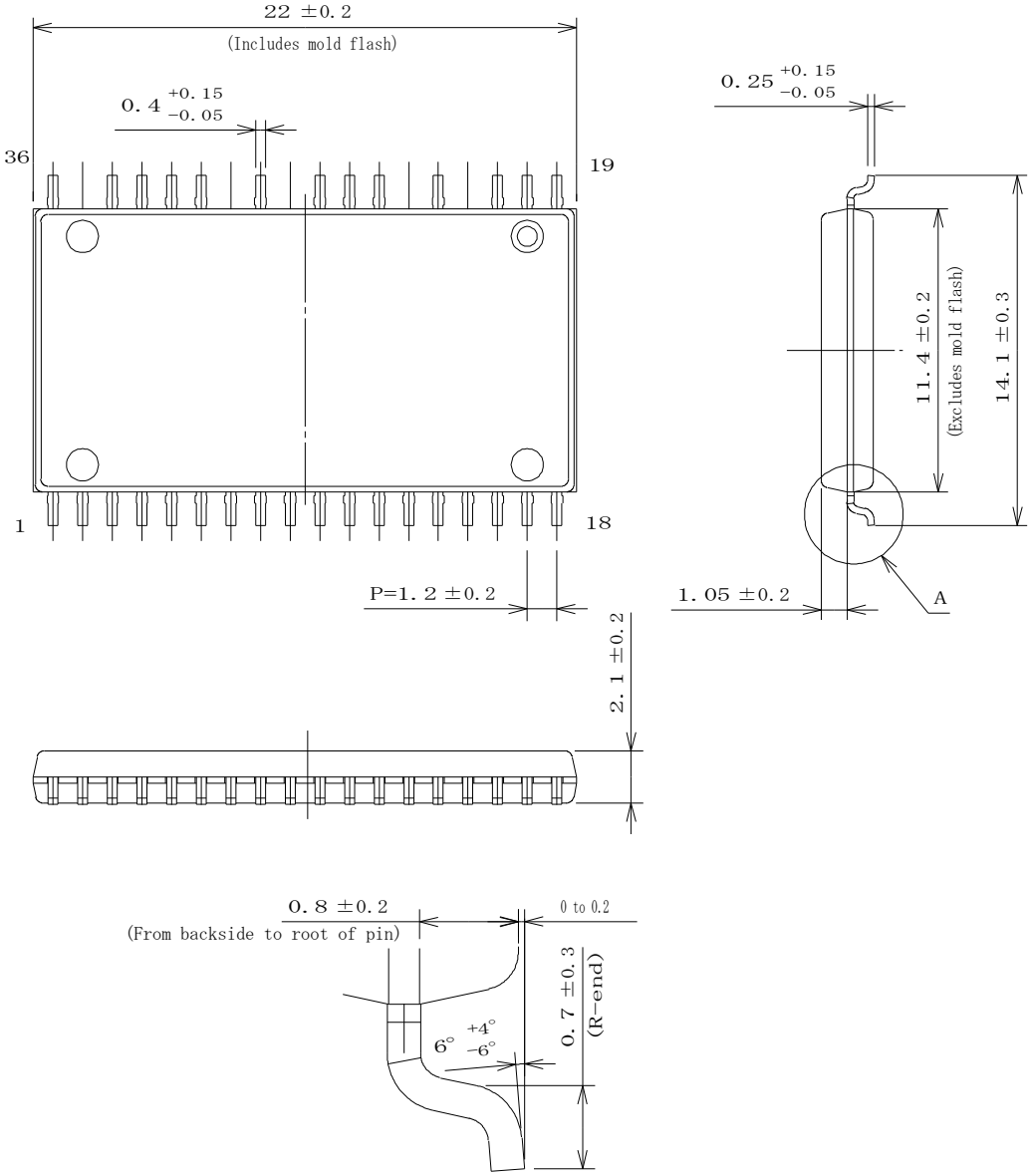


Figure 8-1. Typical Application

9. Physical Dimensions

● **SOP36 Package**

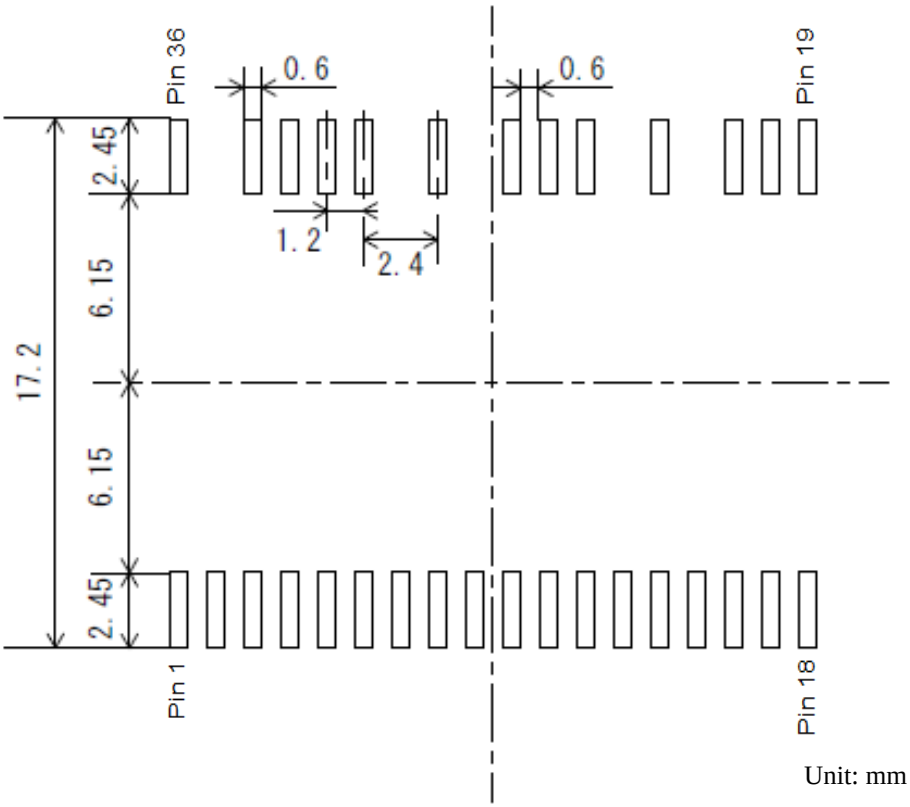


Enlarged view of A (S = 20/1)

NOTES:

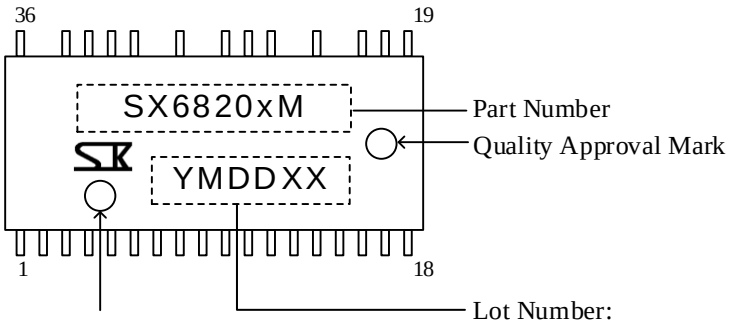
- Dimensions in millimeters
- Pb-free (RoHS compliant)
- When soldering the products, it is required to minimize the working time within the following limits:
  Reflow (MSL3):
  Preheating: 180 °C / 90 ± 30 s
  Solder heating: 250 °C / 10 ± 1 s (260 °C peak, 2 times)
  Soldering iron: 380 ± 10 °C / 3.5 ± 0.5 s, 1 time

● **Land Pattern Example**



Unit: mm

10. Marking Diagram



11. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.

11.1. Basic Operation

The IC is a 3-phase brushless motor driver operated with sinusoidal current waveforms, where the rotor position is estimated by a sensorless vector control strategy. The rotor positioning system is based on calculations from the voltages applied to the 3-phase motor and the currents through each phase, thus requiring no external position sensor. The internal power MOSFETs consisting of 3-phase bridges supply the currents to the motor. The serial communications feature provides reliable access to the extensive collection of settings pertaining to control systems and diagnostic features. The IC integrates a non-volatile memory (EEPROM), which stores register data, to operate independently of external communications.

The IC has the motor speed control system whose reference speed settings are programmable through the serial communications or by an analog voltage input. In an overcurrent condition, the IC puts a certain limit on the motor current level with its protection function.

The startup operation uses the parameters settable via the serial communications, thus permitting the IC to support a wide range of the combinations of motors and loads. Moreover, the built-in watchdog timer allows the IC to stop the present motor run as the protection against chip-level damage, e.g., a control part in a freeze state.

The fault detection and diagnosis on operational faults such as the VCCx or V3 pin undervoltage protection, thermal shutdown, and so on are carried out based on the detailed diagnostic information accessible through the serial communications. The DIAG pin operates as the fault signal output, whose settings are also programmable by the diagnostic register.

For thorough functional descriptions, see the following sections.

11.2. Pin Descriptions

11.2.1. VCC1 and VCC2

These are the logic supply pins for the built-in control ICs. The VCCx pin voltage is used for charging bootstrap capacitors. In addition, the VCCx pin voltage is internally stepped down (i.e., V3 regulator) to be used as a logic power supply. A 26 V Zener diode is internally connected between the VCCx and COM pins.

The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a capacitor of about 0.01 µF to 0.22 µF, C_{VCC}, near these pins. Voltages to be applied between the VCCx and COM pins should be about 15 V.

11.2.2. RESETn

This pin operates to reset the diagnostic register. When the RESETn pin becomes logic low, the motor operation stops, and the diagnostic register is cleared. Then, the DIAG pin is reset to logic high.

The RESETn pin is internally pulled up to the V3 regulator by the resistor. The RESETn pin should be normally left open.

If any noise-induced malfunction occurs, add R_{RST} and C_{RST} as shown in Figure 11-1. When turning on the IC, be sure to check that the RESETn pin is held at logic low. In particular, when applying an external voltage on the RESETn pin, be sure to set the RESETn pin to logic low until the V3 pin voltage is established.

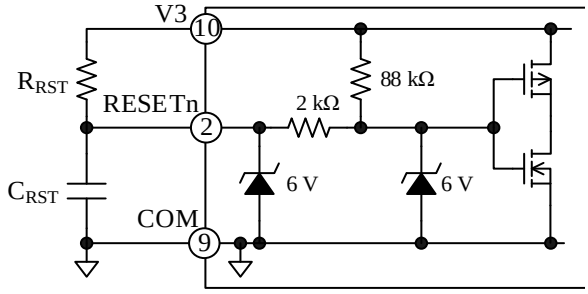


Figure 11-1. Internal Circuit Diagram of RESETn Pin

11.2.3. DIR

This is the signal input pin to switch the direction of motor rotation. The motor direction is determined by the logical EXOR (exclusive OR) of the DIR bit in the internal register and the DIR logic input, as in Table 11-1.

Table 11-1. Logic Levels Defined for Motor Direction

DIR Bit	DIR Pin	Motor Direction
0	L	Forward
0	H	Reverse
1	L	Reverse
1	H	Forward

The DIR pin is internally pulled down to the COM pin with the internal resistor. To set the DIR pin to logic low, normally leave the pin open. If any noise-induced malfunction occurs, connect the DIR pin to the COM pin.

To set the DIR pin to logic high, pull up the pin to the V3 pin with R_{DIR}, as shown in Figure 11-2. If any noise-induced malfunction occurs, add C_{DIR} between the DIR and COM pins.

When turning on the IC, be sure to check that the DIR pin is held at logic low. In particular, when applying an external voltage on the DIR pin, be sure to set the DIR pin to logic low until the V3 pin voltage is established. Note that the motor operation must be stopped for switching the logic level of input signals to the DIR pin.

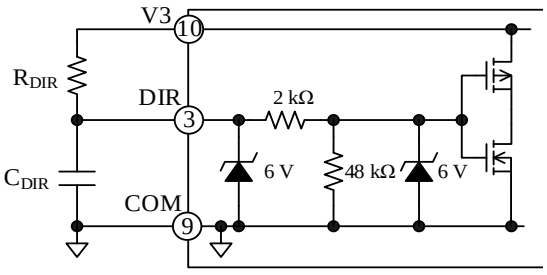


Figure 11-2. Internal Circuit Diagram of DIR Pin

11.2.4. VSP

This is the input pin of reference voltage to set the speed of motor rotation. Figure 11-3 shows an internal circuit diagram of the VSP pin.

The reference voltage is input between the VSP and COM pins. When the VSP pin is held at logic low for a certain period of time, the IC enters the low power consumption mode.

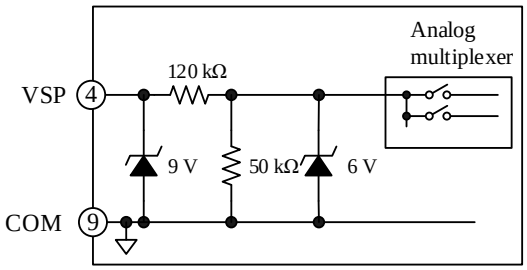


Figure 11-3. Internal Circuit Diagram of VSP Pin

11.2.5. VM

This pin monitors the motor driving voltage, V_{DC}. V_{DC} divided by a resistive voltage divider is applied to the VM pin. Figure 11-4 illustrates an internal circuit diagram of the VM pin.

The resistor should be set within the range specified as the absolute maximum rating (−0.3 V to 4 V). The VM pin also has the overvoltage protection and the undervoltage lockout. For more details, see Section 11.15.4.

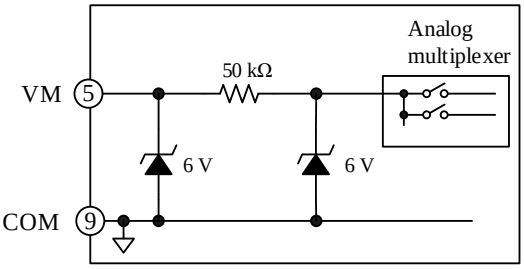


Figure 11-4. Internal Circuit Diagram of VM Pin

11.2.6. TEST

This is the input pin designed for test use only, not for motor control. When using the TEST pin in your application, leave the pin open or connect a resistor of about 10 kΩ between the pin and the ground (COM).

If you have any questions about using the TEST pin, please contact our sales representative or distributor.

11.2.7. SCL

This pin operates as the clock input pin for the serial communications. Figure 11-5 is an internal circuit diagram describing the SCL pin.

While the serial communications are being performed, the power supply (3.3 V to 5.0 V) of the master device must be used. Care must be taken in supplying power to the subordinate and master devices. Be sure to turn on the IC (subordinate) first, and then turn on the master device. The SCL pin should be normally left open.

If any noise-induced malfunction occurs, add R_{SCL} and C_{SCL} as shown in Figure 11-5.

When turning on the IC, be sure to check that the SCL pin is held at logic low.

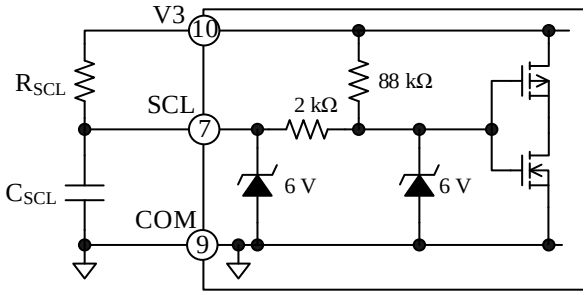


Figure 11-5. Internal Circuit Diagram of SCL Pin

11.2.8. SDA

This is the data input/output pin for the serial communications. Figure 11-6 is an internal circuit diagram describing the SDA pin.

While the serial communications are being performed, the power supply (3.3 V to 5.0 V) of the master device must be used. Care must be taken in supplying power to the subordinate and master devices. Be sure to turn on the IC (subordinate) first, and then turn on the master device. When turning on the IC, be sure to check that the SDA pin is held at logic low.

The SDA pin should be normally left open. If any noise-induced malfunction occurs, connect a resistor of about 10 kΩ between the SDA and COM pins.

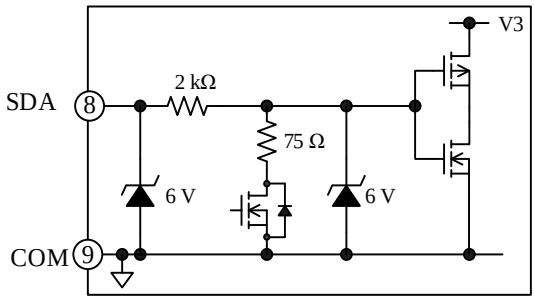


Figure 11-6. Internal Circuit Diagram of SDA Pin

11.2.9. COM

This is the logic ground pin for the built-in control ICs. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to shunt resistors, R_{Sx}, at a single-point ground (or star ground) which is separated from the power ground (see Figure 11-7).

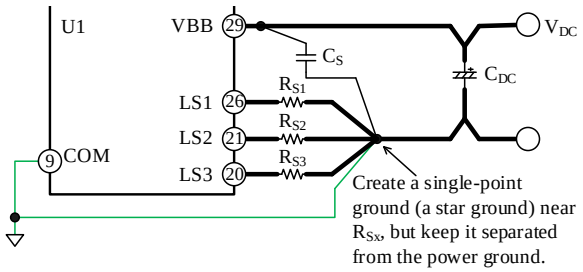


Figure 11-7. Connections to Logic Ground

11.2.10. V3

This pin is the output of the 3.3 V internal regulator. A 6 V Zener diode is internally connected to the V3 pin. Connect a capacitor of about 1.0 µF (≥0.47 µF) between the V3 and COM pins.

11.2.11. VPP

This pin is the input of the programming voltage supply. Writing to the EEPROM requires a programming voltage; therefore, connect a capacitor, C_{VPP}, of about 0.1 µF and apply a voltage of 24 V to it. The IC uses the VPP pin voltage smoothed by the internal regulator. A 30 V Zener diode is internally connected to the VPP pin. When not using the VPP pin, connect the pin to the VCCx or COM pin (no C_{VPP} required).

11.2.12. FG

While internal signals of the IC and the motor rotation synchronizes, the FG pin outputs pulses proportionally to a preset motor electrical cycle frequency. The pulse frequency of the FG pin output is set ×1 or ×3 of the motor electrical cycle frequency by the FGS bit in the configuration register 8 (Config 8). Figure 11-8 shows an internal circuit diagram of the FG pin

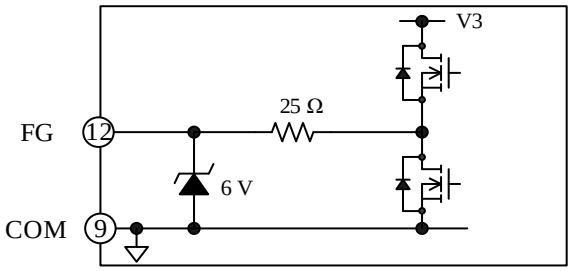


Figure 11-8. Internal Circuit Diagram of FG Pin

11.2.13. DIAG

The DIAG pin outputs fault signals. Figure 11-9 is an internal circuit diagram illustrating the DIAG pin.

For more details, see Section 11.14.1.

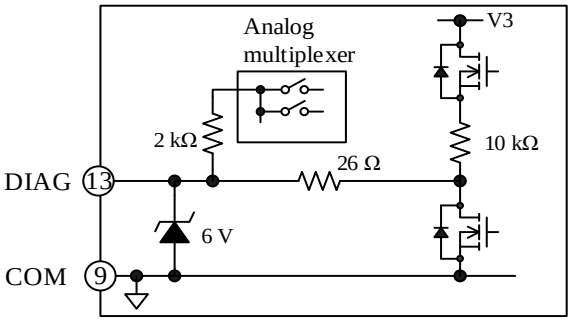


Figure 11-9. Internal Circuit Diagram of DIAG Pin

11.2.14. CSCOM

This pin serves as the reference input for current detection. Connect the CSCOM pin as close as possible to shunt resistors, R_{Sx}, whose traces are separated from the common ground.

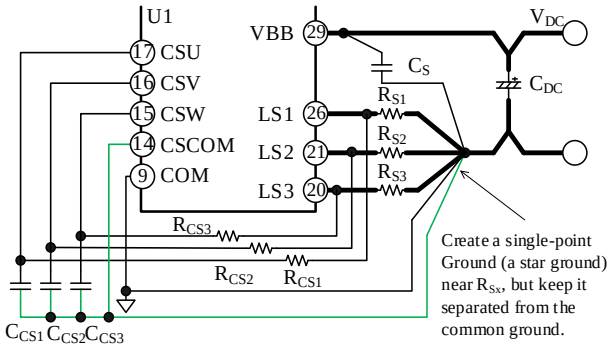


Figure 11-10. Connections to CSCOM Pin

11.2.15. CSU, CSV, and CSW

This is the input pin of current detection signals. Figure 11-11 illustrates an internal circuit diagram of the CSx and CSCOM pins.

The CSU, CSV, and CSW pins are, directly but separately, connected to each current detection resistor of the U-, V-, and W-phases. To eliminate signal ringing which may be induced by parasitic capacitance and the impedance in the detection resistors, add an RC low pass filter (i.e., R_{CSx} and C_{CSx} in Figure 11-10) as needed.

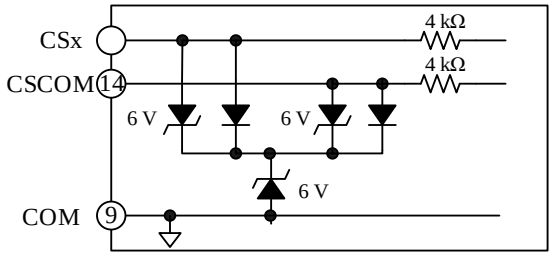


Figure 11-11. Internal Circuit of CSx and CSCOM Pins

11.2.16. VBB

This is the input pin for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to this pin. Voltages between the VBB pin and the ground (COM) should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

To suppress surge voltages, put a 0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBB pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBB pin.

11.2.17. VB1, VB2, and VB3

The VB1, VB2, and VB3 pins are connected to bootstrap capacitors, C_{Bx}, for the high-side floating supply. For proper startup, turn on the low-side transistors first, then fully charge the bootstrap capacitors, C_{Bx}. Section 11.4 describes the startup sequences of the IC in detail; Section 11.12 explains the procedures to charge the bootstrap capacitors.

C_{Bx} of about 1 µF must be placed near the IC, and connected between the VBx and output (U, V1, W1) pins with a minimal length of traces.

11.2.18. U, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively. The U, V, and W1 pins are the grounds for the VB1, VB2, and VB3 pins. The U, V1, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{Bx}. Since high voltages are applied to these output pins (U, V1, V2, W1, W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

11.2.19. LS1, LS2, and LS3

The LS1, LS2, and LS3 pins are internally connected to the low-side power MOSFET sources of the U-, V-, and W-phases, respectively. For current detection, the LSx pin should be externally connected to shunt resistors, R_{Sx}. When connecting a shunt resistor, use a resistor with low inductance (required), and place it as near as possible to the IC with a minimum length of traces to the LSx and COM pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RSx}, between the LSx and COM pins in order to prevent the IC from malfunctioning (see Figure 11-12).

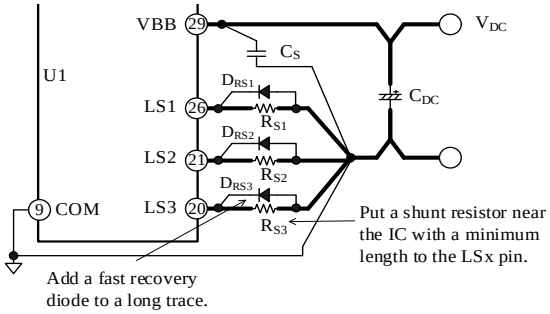


Figure 11-12. Connections to LSx Pin

11.3. Closed-loop Speed Control

In addition to the vector control system, which is a core element in the control systems, the IC also incorporates a closed-loop speed control. The closed-loop speed control uses a preset reference speed as a target motor speed, determined by a frequency of the 3-phase waveforms (an electrical angle of 360°). The reference speed, f_{REF}, is input by either of the following two methods (for the motor speed setting, see Section 11.7):

- Directly inputting the relevant parameter via the serial communications
- Inputting the linear voltage that is proportional to the motor speed into the VSP pin

The reference speed, f_{REF}, and the feedback speed, f_{FBK}, are compared inside the IC to obtain a speed difference, f_{ERR}. f_{ERR} is then fed into the integrating controller to calculate a reference driving torque used for accelerating or decelerating the motor.

The following bits are for setting the speed control method, reference speed range, and the reference speed, respectively:

- Config 15
  SCS Speed control method selection
  SU[3:0] Speed range multiplier
- Config 16
  SR[9:0] Reference motor speed

The integral gain, K_I, used for the speed control is can be adjusted to yield optimum performance by using the SI variable. The rotational inertia of motor load shaft and the desired mechanical response speed determine the SI variable. The following bit is for the SI variable setting:

- Config 8
  SI[3:0] Integral gain constant, K_I, for speed control

11.4. Startup

For proper startup, apply voltages to the main power supply of the motor, the VCC pin, and the VSP pin, in that order. The motor starts to operate with the startup sequence (defined below) depending on the VSP pin voltage levels.

Figure 11-13 explains the startup sequence; Table 11-2 provides the operation modes definitions.

The IC has two startup modes: the DC alignment start mode and the ramp-up start mode. The STM bit in the Run register (Register 31) selects which mode to be enabled. Note that the motor may still be coasting or may be forced to rotate by the operation of a motor load before the startup. Therefore, either of the two startup modes requires the motor to be as stationary as possible in its very first stage. To apply a braking force to the stop the motor, the IC increases the duty cycle of a predetermined PWM period and turns on all the low-side power MOSFETs. During this braking operation, the IC monitors and limits the currents through the motor. The braking force maximizes at the duty cycle increased up to 100%. When the current detected reaches zero, the braking operation completes. The operations after the braking operation are as follows:

- **DC Alignment Start Mode**

As soon as the braking period ends, the direct current of a preset value flows through the motor coil for a predefined hold time. The direct current increases from zero to a maximum value (i.e., the hold current) and remains in this condition for the hold time. This allows the rotor to be aligned to an initial position. In the DC alignment start mode, the hold time and hold current must be large enough to align the rotor to the initial position.

After the hold time ends, the motor rotates at a constant speed which is controlled with a PWM duty cycle generated by the closed-loop speed control system. The initial value of the PWM duty cycle must be set to generate an average voltage equal to the BEMF amplitude at the startup speed.

- **Ramp-up Start Mode**

The ramp-up start mode operation follows the braking period. During the period internally set to about 5 seconds, the excitation switching speed of phase currents gradually increases from 25% to 100% of the start speed (this is defined as a ramp-up period). During the ramp-up period, the rotor position is controlled without feedback. When the excitation switching speed reaches the maximum startup speed, the IC estimates a rotor position by its internal circuits.

After the ramp-up period ends, the motor rotates at a constant speed which is controlled with a PWM duty cycle generated by the closed-loop speed control system. In the ramp-up start mode, the startup speed mainly depends on the rotational inertia and load of the motor. The ramp-up current generates a rotating force, which must be large enough to overcome static friction and rotate the rotor at the startup speed.

The startup parameters are also programmable via the serial communications. The user-settable bits in the configuration registers are as follows:

- Register 31 (Run)
  STM Startup mode selection
- Config 8
  HR[3:0] Startup ramp-up period
- Conig 4
  HT[5:0] Startup hold time
  HD[3:0] Startup hold current
- Config 5
  STS[4:0] Startup speed
  STD[4:0] Startup duty cycle/ramp-up current

To turn off the IC, be sure to decrease the VSP pin voltage first.

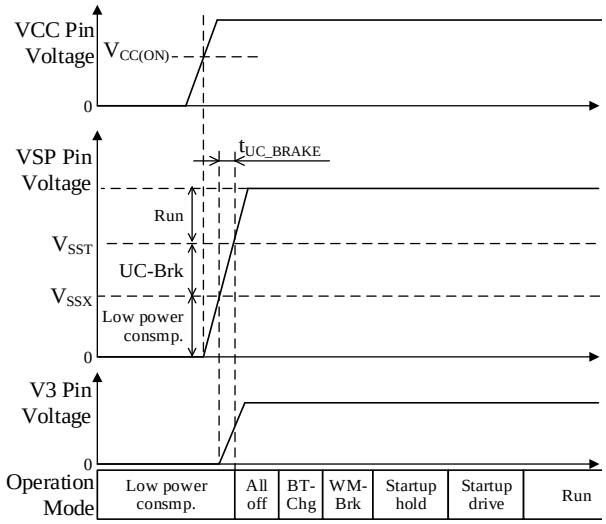


Figure 11-13. Startup Sequence

Table 11-2. Operation Modes in Startup Sequence

Operation Mode	Description
UC-Brk*	The braking operation when the VSP pin voltage is set within the UC-Brk voltage range (UC-Brk: User Commanded Brake)
ALL OFF	Initializing
BT-Chg	Charging the bootstrap capacitors (BT-Chg: Bootstrap Charge)
WM-Brk	The braking operation prior to excitation start (WM-Brk: Windmill Brake)
Startup hold	Aligning the rotor to initial position
Startup drive	Rotating (without feedback)
RUN	Rotating

* At startup, the VSP pin voltage crosses over the voltage range specified for the UC-Brk operation. However, when t_{UC_BRAKE} is shorter than about 200 ms, the UC-Brk operation is skipped.

11.5. Windmilling

In the application where a BLDC motor drives a fan, the startup failure may occur if a motor shaft rotates before the IC attempts the startup sequence. To avoid such failure, the IC performs the braking operation (WM-Brk) prior to the startup sequence to bring the motor to a standstill.

When the WM-Brk operation starts, the duty cycle of the low-side power MOSFETs will gradually increase. The windmill braking current gradually rises with an increase in the duty cycle. The low-side duty cycle increases up to the level where the current reaches a limiting value. The IWM[1:0] bits in the configuration register 3 (Config 3) are for setting a limiting value of the windmill braking current.

The motor BEMF lowers with a decrease in the motor speed induced by the windmill braking current. Eventually, the motor BEMF becomes too low to maintain the windmill braking current even with the low-side power MOSFETs at a 100% duty cycle, and then the windmill braking current decreases. The motor is considered to be stopped as the windmill braking current falls below its minimum threshold. The XWM[1:0] bits in the configuration register 13 (Config 13) are for setting the minimum threshold of the windmill braking current.

After the motor stops, the IC starts the startup sequence.

11.6. Motor Control

The motor running state is controlled by a combination of the register bits set via the serial communications. The Run register (Register 31) contains the following four bits to control motor operations: RUN, DIR, BRK, and RCS.

- **Motor Start/Stop**

The RUN bit receives the signals that start and stop a motor run. When RUN = 1, the IC enters an operating state and starts a motor run or the startup sequence. When RUN = 0, the IC turns off the power MOSFETs of the three phases and allows the motor to coast (i.e., coast mode). This state overrides all other control inputs; therefore, neither the motor run nor the startup sequence takes place.

- **Motor Direction**

Table 11-3 is the logical EXOR (exclusive OR) truth table defining the DIR bit statuses and the logic input levels of the DIR pin, which determine the direction of motor rotation. In a forward rotation, 3-phase currents I_U, I_V, and I_W are 120° ahead of the currents I_V, I_W, and I_U, respectively. In a reverse rotation, 3-phase currents I_U, I_V, and I_W are 120° behind the currents I_V, I_W, and I_U, respectively.

Table 11-3. Motor Direction Definitions

DIR Bit	DIR Pin	Motor Direction
0	L	Forward
0	H	Reverse
1	L	Reverse
1	H	Forward

● **Braking Operation**

The BRK bit controls the braking operation, which decelerates the speed of motor rotation to stop the motor run. The braking operation is enabled only when RUN = 1. During the braking operation, all the low-side power MOSFETs turn on to short the motor windings. The rotation-induced BEMF causes currents to flow through the motor winding of each phase. And this generates a braking torque. The braking torque always opposes the motor direction. Strength of the braking torque varies according to the motor parameters. Note that the current control is not available during the braking operation due to no excitation exerted on the motor. Be sure to maintain the braking current not to exceed the rating of the low-side power MOSFETs.

● **Motor Speed**

The voltage applied to the VSP pin is used for the motor speed setting (see Section 11.7). The motor speed can be determined by monitoring the FG pin output. While the IC drives under the sensorless control system, the FG pin outputs pulses at a frequency proportional to the motor speed.

● **Loss of Synchronization**

While the motor is in a running state, the IC monitors a loss-of-synchronization (LOS) condition. Upon LOS detection, the LOS bit in the diagnostic register is set to "1". When the motor is not in the running state or when in the braking state, the LOS bit is set to "0".

11.7. Motor Speed Setting

The IC controls the speed of motor rotation with the built-in closed-loop speed control circuit. To enable a motor run, set BRK = 0 and RUN = 1. The SCS bit in the configuration register 15 (Config 15) selects either of the following speed control methods:

- SCS = 1
  Controlled by the internal register settings (directly input the SR parameter via the serial communications)
- SCS = 0
  Controlled by externally inputting the linear voltage proportional to the motor speed into the VSP pin (external mode)

When SCS = 1, the parameter is directly input via the serial communications. The IC then ignores the VSP pin input but only uses the value input to the SR[9:0] bits in the configuration register 16 (Config 16). The SR[9:0] bits are for setting the frequency of motor excitation.

When SCS = 0, the IC uses the value of the voltage applied to the VSP pin as a default value. Figure 11-14 shows a relation between the reference motor speed and the VSP pin input voltage. The relation between the VSP pin voltage and the motor speed is defined by the six variable parameters (listed in Table 11-4) and an internally fixed voltage, V_{SSX}.

V_{SSX} represents the releasing voltage of the low power consumption mode, i.e., a voltage of an internally preset value.

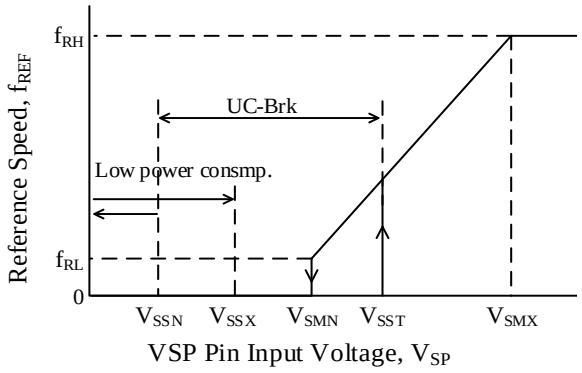


Figure 11-14. Reference Speed, f_{REF} vs. VSP Pin Input Voltage, V_{SP}

Table 11-4. VSP Input Register

Variable	Symbol	Description
VX[9:0]	V_{SMX}	VSP pin voltage at maximum speed
VN[9:0]	V_{SMN}	VSP pin voltage at minimum speed
VS[9:0]	V_{SST}	Excitation start voltage
VC[9:0]	V_{SSN}	Low power consumption mode transition voltage
SRH[9:0]	f_{RH}	Maximum reference speed
SRL[9:0]	f_{RL}	Minimum reference speed

When the VSP pin input voltage, V_{SP}, reaches zero, the IC turns off the power MOSFETs of the three phases and allows the motor to coast. Then, the IC enters the low power consumption mode (see Section 11.8). When $V_{SP} \leq V_{SSX}$, the IC stays in the low power consumption mode. When $V_{SP} > V_{SSX}$, the IC is initialized and goes into a braking operation state (shown in Figure 11-13).

When the IC shifts into the braking operation state from the low power consumption mode, the power MOSFETs of the three phases are held turned off until the IC initialization completes. The braking operation (UC-Brk) continues until V_{SP} rises above the excitation start voltage, V_{SST}. When $V_{SP} > V_{SST}$, the IC enters in a running state (Run mode) and starts the startup sequence. The motor is controlled according to the f_{REF} vs. V_{SP} relationship, as described in Figure 11-14. And this relationship is determined by V_{SMN} and V_{SMX}, representing the VSP input voltages at minimum and maximum speeds, respectively.

f_{RL} and f_{RH}, representing minimum and maximum reference speeds, are defined by the SRL, SRH, and SU parameters set in the configuration registers (Config 15

to 17). f_{RL} and f_{RH} are given by the following equations using these parameters:

$$f_{RL} = SRL \times SU \times 0.1\ (Hz)\ , \text{and} \quad (1)$$

$$f_{RH} = SRH \times SU \times 0.1\ (Hz)\ . \quad (2)$$

Where $V_{SP} = V_{SMN}$ and $f_{REF} = f_{RL}$.

The f_{REF} vs. V_{SP} relationship is then defined as:

$$f_{REF} = (S \times V_{SP}) + Z\ . \quad (3)$$

Where Z is obtained by:

$$Z = f_{RH} - (V_{SMX} \times S)\ . \quad (4)$$

Let S be the motor speed given by:

$$S = \frac{(f_{RH} - f_{RL})}{V_{SMX} - V_{SMN}}\ . \quad (5)$$

The actual motor speed, S, depends on the number of pole pairs in the rotor, N_{PP}, as defined by:

$$S = \frac{(f_{REF} \times 60)}{N_{PP}}\ . \quad (6)$$

Here, f_{REF} is in Hz and S is in rpm.

Once the motor starts running, the f_{REF} vs. V_{SP} relationship is valid for all the V_{SP} values that fall into the range between V_{SMN} and V_{SMX}. In the range where $V_{SP} > V_{SMX}$, the motor speed is always determined by f_{RH}. The motor continues running until V_{SP} becomes lower than V_{SMN}.

11.8. Low Power Consumption Mode

The IC incorporates the low power consumption mode function. When the VSP pin voltage, V_{SP}, remains at a voltage not exceeding the lower power consumption mode transition voltage, V_{SSN}, for a certain time, the IC transits to the low power consumption mode. In the low power consumption mode, the IC suppresses the VCCx pin supply current as much as possible by clearing the fault flags set by the diagnostic register and by stopping the internal circuit operations. To return from the low power consumption mode, hold the outputs with off status by the protection until the IC initialization completed.

Note that V_{SSN} must be set to a voltage lower than the releasing voltage, V_{SSX}; otherwise, V_{SSN} will have no effect. In the case where V_{SSN} is set to a voltage higher than V_{SSX}, the IC ignores the V_{SSN} setting and enters the low power consumption mode even when $V_{SP} \leq V_{SSX}$.

11.9. PWM Control

The PWM generator built in the IC provides all the timings associated with the PWM control of motor currents through the internal MOSFETs. The PWM generator also controls PWM frequency, duty cycle, dead time, and current sampling time. PWM signals of the three phases have the same frequency but have independent duty cycles. Note that switching loss, audible noise, and duty cycle accuracy must be taken into account in setting a PWM frequency.

The PR[7:0] bits in the configuration register 0 (Config 0) are for setting a PWM period for all the three phases. These 8 bits contain a positive integer. The PWM period can be adjusted in units of 8 cycles of the system clock. The equation below defines the PWM period, T_{PR}:

$$T_{PR}\ (\mu s) = 30.5 + (n \times 0.4)\ . \quad (7)$$

Where n is a positive integer determined by the PR[7:0] bits. For example, when PR[7:0] = [0100 0111] (i.e., 71 in decimal) then T_{PR} = 58.9 µs (typ.).

11.10. Dead Time

In case any high-side power MOSFET of the three phases and the corresponding low-side power MOSFET turn on at the same time, a short-circuit condition may occur. For protecting all the 3-phase power MOSFETs from such abnormal condition, a dead time must be set between a turn-off of each high- or low-side power MOSFET and the next turn-on of its pairing low- or high-side power MOSFET.

The DT[5:0] bits in the configuration register 1 (Config 1) are for setting a dead time for the three phases. Be sure to set the t_{DEAD} so that it falls within the recommended operating range (i.e., ≥1.5 µs).The equation below defines the dead time, t_{DEAD}:

$$t_{DEAD} = n \times 50\ ns\ . \quad (8)$$

Where n is a positive integer determined by the DT[5:0] bits. A minimal value of t_{DEAD} is 100 ns. For example, when DT[5:0] = [01 1110] (i.e., 30 in decimal) then t_{DEAD} = 1.5 µs (typ.).

11.11. PWM Switching Mode

The IC has the following four PWM switching modes. The 2-phase PWM switching mode decreases switching loss by about 33% but results in less-accurate phase current at low motor speed. In general, therefore, operating the IC at lower speed and current requires the 3-phase PWM switching mode, whereas operating the IC at higher speed and current demands the 2-phase PWM switching mode.

The CMS[1:0] bits in the configuration register (Config 2) is for setting which mode to be enabled.

- CMS[1:0] = [00]: 2-phase PWM switching
- CMS[1:0] = [01]: 3-phase switching
- CMS[1:0] = [10]:
  IC operation shifts from 3-phase to 2-phase switching at a modulation index of ≥50%. IC operathion shifts back to the 3-phase switching at a modulation index of <50%.
- CMS[1:0] = [11]:
  IC operation shifts from 3-phase to 2-phase PWM switching at a modulation index of ≥50%. IC operation shifts back to 3-phase PWM switching at a modulation index of <25%.

11.12. Charging of Bootstrap Capacitors

To start up the IC properly, turn on the low-side power MOSFETs first and fully charge bootstrap capacitors. The BCG[2:0] bits in the configuration register 3 (Config 3) are for setting the charging time of bootstrap capacitors, t_{BCG}. t_{BCG} should range from 1 ms to 100 ms. When BCG[2:0] = 0, the charging operation is disabled.

11.13. Current Detection

Current detection resistors, R_{Sx}, should be connected between the low-side power MOSFET sources and the ground. This connection allows only phase currents to flow through the current detection resistors when the low-side power MOSFETs turn on. Which means that currents are detectable only when the low-side power MOSFETs are on. Section 11.2.15 describes the pins used for current detection, the CSU, CSV, and CSW pins. Section 11.2.14 gives details on the CSCOM pin used as the reference input for current detection.

The PWM generator produces a current detection signal for each phase at the timing of the midpoint of each low-side power MOSFET on-time. To detect stable currents, the IC needs a certain period of on-time (i.e., minimum on-time) from a turn-on of the low-side power MOSFET until when currents are settled. If a low-side on-time is too short to allow currents to settle in time, the IC fails to perform current sampling. The minimum on-time for current detection can be set through the serial communications. The MO[3:0] bits in the configuration register 3 (Config 3) are for setting the minimum on-time. These 4 bits contain a positive integer. The equation below defines the minimum on-time, t_{MO}:

$$t_{MO} = n \times 400\ \text{ns}\,. \tag{9}$$

Where n is a positive integer determined by the MO[3:0] bits. For example, when MO[3:0] = [1010] (i.e., 10 in decimal) then t_{MO} = 4.0 µs (typ.).

When an RC filter is added to the input side of the current-sensing operational amplifier, an additional delay time will occur due to filtering. The timing of current detection can be delayed from the midpoint of an on-time produced by the PWM generator. The CD[3:0] bits in the configuration register 2 (Config 2) are for setting the current detection delay time, t_{CD}.

The equation below defines the current detection delay time, t_{CD}:

$$t_{CD} = n \times 200\ \text{ns}\,. \tag{10}$$

Where n is a positive integer determined by the CD[3:0] bits. For example, when CD[3:0] = [0101] (i.e., 5 in decimal) then t_{CD} = 1.0 µs (typ.).

The IC detects a phase current with the voltage across the current detection resistor, R_{Sx}. The current-sensing operational amplifier has the four input voltage ranges selectable by the CR[1:0] bits in the configuration register 0 (Config 0). Table 11-5 shows the maximum input voltage ranges defined for the current-sensing operational amplifier, with the corresponding maximum current ranges, I_{FS}. Table 11-6 lists resistances in the maximum input voltage ranges, with the corresponding current ranges as examples.

The maximum operating current, I_{MX}, is a limitation value of a target current required for the closed-loop speed control. When the current needed for the speed control exceeds I_{MX}, the IC fails to maintain the speed control due to the current limitation.

I_{MX} is expressed as a percentage of the maximum current range, I_{FS}. The equation below defines I_{MX}:

$$I_{MX} = [38 + (n \times 2)](\%) \times I_{FS}\,. \tag{11}$$

Where n is a positive integer determined by the IM[4:0] bits in the configuration register 7 (Config 7). For example, when IM[4:0] = [0 0110] (i.e., 6 in decimal) then I_{MX} = 50% I_{FS}. I_{MX} should range from 38% to 100% of I_{FS}.

Table 11-5. Maximum Input Ranges for Current-sensing Operational Amplifier

CR1	CR0	Maximum Input Voltage Range (mV)	Maximum Current Range, I_{FS} (A)
0	1	−500 to 500	±500 / R_S
0	0	−250 to 250	±250 / R_S
1	1	−125 to 125	±125 / R_S
1	0	−62.5 to 62.5	±62.5 / R_S

R_S represents a resistance of R_{Sx}, measured in mΩ.

Table 11-6. Current Range vs. Example Sensing Resistor

R_S (mΩ)	Maximum Current Range, I_{FS} (A)	Accuracy (mA)	P_{LOSS} (W)
CR[1:0] = [00] (Input Voltage Range ± 500 mV)			
100	−5 to 5	±25	2.50
200	−2.5 to 2.5	±13	1.25
500	−1 to 1	±5	0.50
1000	−0.5 to 0.5	±3	0.25
CR[1:0] = [01] (Input Voltage Range ± 250 mV)			
40	−6.3 to 6.3	±31	1.56
100	−2.5 to 2.5	±13	0.63
200	−1.3 to 1.3	±6	0.31
500	−0.5 to 0.5	±3	0.13
CR[1:0] = [10] (Input Voltage Range ± 125 mV)			
10	−12.5 to 12.5	±63	1.56
20	−6.3 to 6.3	±31	0.79
50	−2.5 to 2.5	±13	0.31
100	−1.3 to 1.3	±6	0.17
CR[1:0] = [11] (Input Voltage Range ± 62.5 mV)			
2	−31.3 to 31.3	±156	1.95
5	−12.5 to 12.5	±63	0.78
10	−6.3 to 6.3	±31	0.39
50	−1.3 to 1.3	±6	0.08

11.14. Diagnostic Function

The IC includes the diagnostic function which indicates a detected fault status. The fault status is available from the following two sources: the DIAG output and the serial interface.

11.14.1. DIAG Pin Output

The DIAG pin outputs a fault signal when the IC detects any fault status and the corresponding fault flag in the diagnostic register is set. When the diagnostic function is disabled by the mask register (Register 29), the DIAG pin outputs no fault signal. However, the DIAG pin outputs a fault signal even when the outputs are off due to a short-circuit condition. The DIAG[4:0] bits in the Registers 30 and 31 define the detailed settings of the DIAG pin output.

The DIAG pin is logic high in normal operation, and is logic low in fault signal output operation.

11.14.2. Diagnostic Register

The detailed diagnostic information contained in the diagnostic register (Register 30) can be read via the serial communications at any time. When a fault status occurs, the corresponding bit in the diagnostic register is set to "1" and is then held in this setting. The fault flag is cleared when either of the following conditions is met:

- When the reading from the diagnostic register completes
- When the RESETn pin is held at logic low for the duration longer than a minimum reset pulse width

When an IC-specific fault state persists even after the diagnostic register is cleared (e.g., when the IC still remains in a high-temperature state), the diagnostic register does not accept the clearing operation and keep the fault flag being set.

The higher 6 bits contained in all the registers, including the diagnostic register, always indicate serious faults (i.e., critical fault flags). Among these bits, the MSB (bit 15) is the FF bit which indicates a common fault flag. The FF bit is set to "1" in either of the following conditions: when any of the bits (except for the EE bit) in the diagnostic register is set; when a write operation via the serial communications fails. The FF bit is cleared only when the fault flag set by the diagnostic register is cleared. The FF bit provides an indication that a fault has occurred since the last fault flag clear.

At power-on or after a power-on reset, the FF and POR bits are set to "1" to indicate a critical fault flag, whereas all other bits in the diagnostic register are cleared. This fault status indicates that a power-on reset has occurred and all the registers are reset to default. Note that only a power-on reset occurs when the V3 pin voltage exceeds the V3 Pin UVP Threshold Voltage, V_{3UV}. The occurrence of a power-on reset is not subject to the VCCx pin voltage level.

11.14.3. Protective Operations at Fault Detection

Table 11-7 lists the fault statuses and the corresponding protective operations at fault detection.

The IC turns off all the power MOSFETs regardless of the ESF bit setting when the IC detects the following faults: V3 pin undervoltage (power-on reset), watchdog timeout, memory error, soft overcurrent, and hard overcurrent.

The EFS bit in the Run register (Register 31) sets which protective operation to be performed when the IC detects the following faults: power module fault, loss of synchronization, and thermal shutdown. When ESF = 1, the IC turns off all the power MOSFETs and allows the motor to coast upon detection of any of the three faults mentioned above. While a soft overcurrent condition is detected, the IC keeps all the power MOSFETs turned off until any of the following conditions is met:

- The RESETn pin becomes logic low
- A serial read operation completes
- A power-on reset occurs

When ESF = 0, the IC never stops its operations even after the diagnostic register has set a fault flag. Consequently, the IC and the motor must be controlled with the master controller or an external circuit to prevent any damage.

Table 11-7. Fault Statuses and Protective Operations

Fault Status	Outputs Disabled		Latched
	ESF = 0	ESF = 1	
No Fault	No	No	—
Power Module Fault	No	Yes*	No
EEPROM Overwrite	No	No	Yes
V3 Pin Undervoltage (POR)	Yes*	Yes*	No
Watchdog Timeout	Yes*	Yes*	Yes
Memory Error	Yes*	Yes*	Yes
Loss of Synchronization	No	Yes*	No
Thermal Warning	No	No	No
Thermal Shutdown	No	Yes*	No
Soft Overcurrent	Yes*	Yes*	Only when ESF = 1
Hard Overcurrent	Yes*	Yes*	Only when ESF = 1
VM Pin Overvoltage	No	Yes*	No
VM Pin Undervoltage	No	Yes*	No

* All the power MOSFETs off.

11.14.4. Fault Mask Setting

The mask register (Register 29) determines which fault status not to be diagnosed (i.e., mask setting). Extreme care must be taken, however, in disabling the individual diagnostic parameters to protect the IC from potentially damaging conditions.

When any given bit in the mask register is set to "1", the corresponding diagnostic parameter is completely disabled. According to the disabled diagnostic parameter, neither fault flag setting nor fault signal output from the DIAG pin takes place. The maskable fault statuses and the corresponding fault mask bits are as follows:

- TW: Thermal warning
- OT: Thermal shutdown
- LOS: Loss of synchronization
- PMF: Power module fault
- HOC: Hard overcurrent
- OVM: VM pin overvoltage
- UVM: VM pin undervoltage

Note that the V3 undervoltage protection cannot be disabled because the accuracy of the diagnostic function and the output control depend on the V3 pin voltage.

11.15. Protection Functions

This section describes the various protections provided in the SX68200M series. The embedded protections monitor the parameters (e.g., V3 pin [regulator] voltage, watchdog timer, driving current) fundamental to drive the IC and the motor reliably and safely.

11.15.1. V3 Pin Undervoltage Protection

The IC monitors the V3 pin voltage, V_3, to ensure its correct logical operation. When V_3 decreases to the V3 Pin UVP Threshold Voltage (V_{3UV} = 2.8 V) or less, all the power MOSFETs turn off immediately. Then, the IC enters a power-down state and stops all the internal operations other than the V3 pin voltage monitoring. When V_3 increases to V_{3UV} + V_{3UVHYS} or more, the IC performs a power-on reset, causing all the configuration registers to be reset to their power-on states. The higher 6 bits contained in all the registers are also cleared at this time. The FF and POR bits are set to "1" to indicate the critical fault flag showing that a power-on reset has occurred. The IC performs the same power-on reset sequence at power-on or V3 brown-out (where only V_3 drops below V_{3UV} momentarily).

11.15.2. Watchdog Timeout

The IC integrates a watchdog timer separated from the internal oscillator. The watchdog timer is a clock which is independent of the main controller system clock, and used for monitoring a latch-up state caused on the main controller. The main controller regularly resets the watchdog counter. When the counter enters a timeout state without clearing, the FF and WD bits are set to "1" to indicate a critical fault flag.

When a watchdog timeout state occurs, the IC turns off all the power MOSFETs and allows the motor to coast because no accurate motor operation is guaranteed. This strategy ensures the safe operations of the internal power MOSFETs and the motor.

The watchdog timeout state persists until the RESETn pin becomes logic low, or a power-on reset occurs.

11.15.3. Memory Error

The IC integrates a non-volatile memory (EEPROM) which stores register data. Each time the active registers are read, the IC verifies the data stored in the EEPROM.

When verifying the stored data, the IC uses additional parity bits to detect a data error. This data check is

performed each time a read from the EEPROM or a copy to the active registers takes place.

When the IC detects a memory error, all the power MOSFETs turn off then the FF and ME bits are set to "1" to indicate a critical fault flag. All the operations other than this protective operation continue as normal.

In case of memory error, turn off the IC first, and then turn on the IC again. This protective operation resets the IC and enables reading the EEPROM data. After the power-on reset, the ME bit is cleared. When the data is then read correctly, the ME bit remains to be cleared. In case a memory error reoccurs after the power-on reset, the active registers must be reset to the correct values via the serial communications. These correct values should be rewritten to the EEPROM to overwrite the previously saved data. After the rewrite operation, the EEPROM should be read and transferred back to the active registers. And this data check sequence permits the IC to recheck the present state of the stored data. When the ME bit is cleared after the data recheck results in no error, the IC continues operating. This state, however, indicates that a soft data error has occurred.

If the ME bit remains set at "1" even after the data recheck, the IC is no longer usable due to a hard error caused by the EEPROM.

11.15.4. Overvoltage Protection and Undervoltage Lockout for Main Power Supply

The IC monitors the Main Supply Voltage, V_{DC}, supplied for driving the motor, with the VM pin to detect an overvoltage or undervoltage condition. V_{DC} divided by a resistive voltage divider is applied to the VM pin.

Along with an increase in V_{DC}, when the VM pin voltage also increases to the VM Pin OVP Threshold Voltage (V_{OVM} = 1.24 V) or more, the FF and OVM bits in the diagnostic register are set to "1". In addition to this state, all the power MOSFETs turn off when ESF = 1.

Along with a decrease in V_{DC}, when the VM pin voltage also decreases to the VM Pin UVP Threshold Voltage (V_{UM} = 0.3 V or 0.6 V) or less, the FF and UVM bits in the diagnostic register are set to "1". In addition to this condition, the IC turns off all the power MOSFETs when ESF = 1. V_{UM} is a user-settable parameter by the UVS bit in the configuration register 8 (Config 8) to 0.3 V or 0.6 V.

11.15.5. Overcurrent Protections

Two overcurrent protections are incorporated in the IC: the soft overcurrent protection and the hard overcurrent protection. Figure 11-15 shows operational waveforms of these functions.

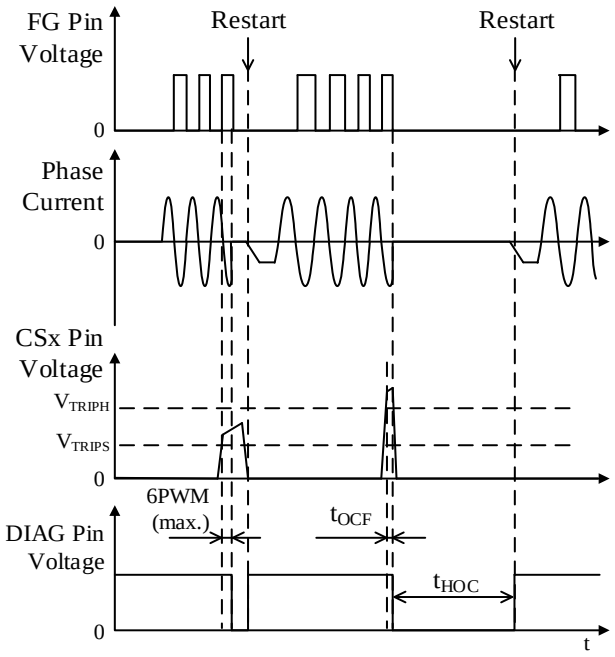


Figure 11-15. Operational Waveforms of SOCP (ESF = 0) and HOCP (ESF = 0, HOC = 0)

11.15.6. Soft Overcurrent Protection

The IC uses a user-settable soft overcurrent threshold current, I_{LIM}, expressed as a percentage of the maximum current range, I_{FS}. The soft overcurrent protection (SOCP) monitors a load short or loop control failure.

When the IC detects a current exceeding I_{LIM}, the FF and OC bits are set to "1" to indicate a critical fault flag and all the power MOSFETs turn off for protecting the motor driving system.

The ESF bit in the Run register determines whether to latch the power MOSFET turn-off operation after the SOCP detection.

When ESF = 1, the IC keeps all the power MOSFETs turned off and the motor stopped (i.e., latch operation) until a restart after the detected error has been eliminated.

When ESF = 0, the IC turns off all the power MOSFETs upon SOCP detection. When phase currents fall below I_{LIM}, the IC restarts to operate.

The equation below defines the SOCP threshold current, I_{LIM}:

$$I_{LIM} = [38 + (n \times 2)](\%) \times I_{FS} . \quad (12)$$

Where n is a positive integer determined by the IO[4:0] bits in the configuration register 7 (Config 7). For example, when IO[4:0] = [1 0101] (i.e., 21 in decimal) then I_{LIM} = 80% I_{FS}.

When IO[4:0] = 0, the SOCP function is disabled. This setting does not protect the internal power MOSFETs and the load; therefore, alternative measures must be taken to protect the IC and the motor from any damage due to large currents.

11.15.7. Hard Overcurrent Protection

The hard overcurrent protection (HOCP) consists of an independent monitoring circuit in order to promptly offer the protection against overcurrents. The HOCP function detects a load short or loop control failure.

When the IC detects a current exceeding the HOCP Threshold Current, I_{HOC}, the IC turns off all the power MOSFETs to protect the motor driving system, and then sets FF and HOC bits in the diagnostic register to "1". Moreover, the IC has a propagation delay of <10 µs between the overcurrent detection to the HOCP activation.

The IHO bit in the configuration register 3 (Config 3) sets I_{HOC}, either to 150% or 200% of the maximum current detection range, I_{FS}.

The HOCP circuit also has a digital low pass filter that avoids itself from responding to an instantaneous overcurrent induced by power MOSFET switching. Thus, the IC does not detect an overcurrent of less than t_{OCF}, 0.5 µs to 2 µs, settable by the OCF[1:0] bits in the configuration register 2 (Config 2).

The ESF bit in the Run register determines whether to latch the power MOSFET turn-off operation after the HOCP detection.

When ESF = 1, the IC keeps all the power MOSFETs turned off and the motor stopped (i.e., latch operation) until a restart after the detected error has been eliminated.

When ESF = 0, the IC turns off all the power MOSFETs for a period of an HOCP hold time, t_{HOC}, upon HOCP detection. The IC then resumes monitoring the currents after a lapse of t_{HOC}. When an HOCP condition is detected again, the IC turns off all the power MOSFETs. After a period of t_{HOC}, the IC restarts monitoring the current. This sequence continues until a stop command is asserted by an external controller. The equation below defines the HOCP hold time, t_{HOC}:

$$t_{HOC} = (1 + n) \times 100 \text{ ms}. \quad (13)$$

Where n is a positive integer determined by the OHT[3:0] bits in the configuration register 1 (Config 1). For example, when OHT[3:0] = [1001] (i.e., 9 in decimal) then t_{HOC} = 1.0 s.

11.15.8. Thermal Warning and Thermal Shutdown

The IC has the thermal shutdown (TSD) circuit for both of the built-in control MIC and gate-drive MIC. The control MIC has two thermal thresholds for the thermal warning and TSD. The gate-drive MIC has one thermal threshold for the TSD. Among these three thermal thresholds, the gate-drive TSD threshold is set to the lowest value. Hence, the IC is basically protected by the TSD of the gate-drive MIC.

When a junction temperature of the gate-drive MIC increases to the gate-drive MIC TSD temperature, T_{DHD} or more, the DIAG pin becomes logic low and the PFM bit in the diagnostic register is set to "1". In addition to this state, all the power MOSFETs turn off when ESF = 1.

When the junction temperature of the gate-drive MIC decreases to $T_{DHD} - T_{DHYSD}$ or less, the DIAG pin becomes logic high. But the state of the PMF bit in the diagnostic register remains unchanged until a reset operation occurs.

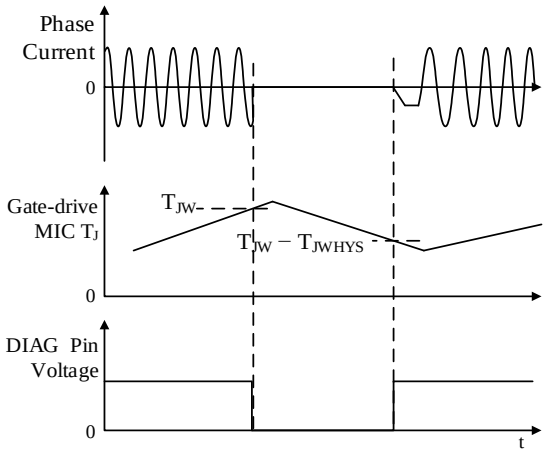


Figure 11-16. TSD Operational Waveforms of Gate-drive MIC (ESF = 1, PMF = 0)

11.15.9. Undervoltage Lockout for Logic Supply

To prevent permanent damage due to an undervoltage condition in the logic power supply, the SX68200M series has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies.

As Figure 11-17 shows, when the voltage between the VBx and output (U, V1, or W1) pins, V_{BS}, decreases to $V_{BS(OFF)}$ or less, the high-side UVLO gets activated and all the power MOSFETs turn off. When V_{BS} increases to $V_{BS(ON)}$ or more after that, the IC restarts to operate. During the high-side UVLO operation, the DIAG pin outputs no fault signals.

As Figure 11-18 shows, when the voltage between the

VCCx and COM pins, V_{CC}, decreases to $V_{CC(OFF)}$ or less, the low-side UVLO gets activated. During the low-side UVLO operation, the PMF bit in the diagnostic register is set to "1" and the DIAG pin becomes logic low. In addition to this condition, the IC turns off all the power MOSFETs when ESF = 1. When V_{CC} increases to $V_{CC(ON)}$ or more after that, the IC restarts to operate.

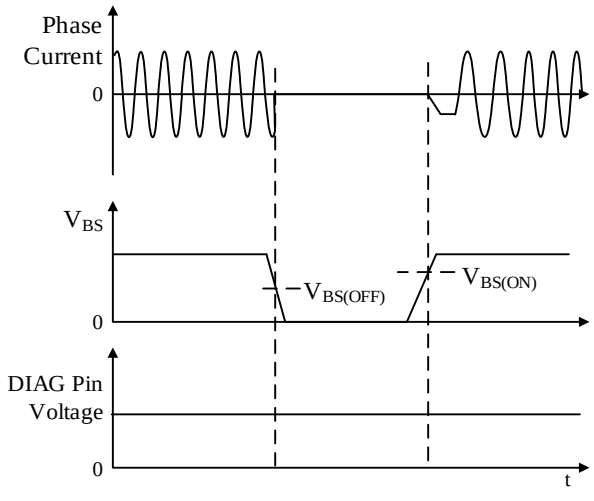


Figure 11-17. High-side UVLO Operational Waveforms

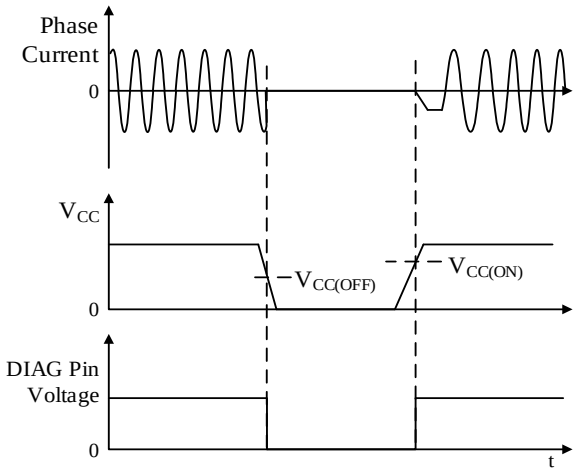


Figure 11-18. Low-side UVLO Operational Waveforms (PMF = 0)

11.15.10. Loss-of-Synchronization Protection

As described in Section 11.3, the IC estimates the motor speed as part of the closed-loop speed control system. The IC recognizes a loss-of-synchronization condition, in which a sensorless signal and a motor rotational frequency are asynchronous, when the estimated speed is lower than a lowest speed threshold, f_{LS}, or higher than a highest speed threshold, f_{HS}.

The LS[5:0] bits and HS[3:0] bits in the configuration register 6 (Config 6) are for setting the lowest and higher speed thresholds, f_{LS} and f_{HS}, respectively.

The equation below defines the lowest speed threshold, f_{LS}:

$$f_{LS} = n \times 0.8 \text{ Hz} . \quad (14)$$

Where n is a positive integer determined by the LS[5:0] bits. For example, when LS[5:0] = [00 0000] (i.e., 0 in decimal) then f_{LS} = 0 Hz. When f_{LS} = 0, the lowest speed detection is disabled.

The equation below defines the highest speed threshold, f_{HS}:

$$f_{HS} = n \times 102.4 \text{ Hz} . \quad (15)$$

Where n is a positive integer determined by the HS[3:0] bits. For example, when HS[3:0] = [0101] (i.e., 5 in decimal) then f_{HS} = 512 Hz.

After the LOS detection, the FF and LOS bits in the diagnostic register are set to "1". When DIAG[4:0] = 0 or 1, the DIAG pin becomes logic low. In addition to this state, all the internal power MOSFETs are turned off (i.e., coast mode) when ESF = 1.

The RSC bit is the reset bit. When RSC = 0, the IC holds the coast mode until a stop command is asserted by an external controller. When RSC = 1, the IC increments a reset counter and starts the startup sequence. When the startup fails and an LOS condition reoccurs, the reset counter is incremented again. And the IC repeats the startup sequence. This operation continues until the reset counter reaches the upper limit number of restarts, determined by the RSN[1:0] bits in the configuration register 2 (Config 2), or until a stop command is asserted. When the reset counter reaches the predetermined upper limit number of resets, the IC holds the coast mode until a stop command is asserted by one of the control inputs. When RSN[1:0] = [11], the IC repeats the startup sequence indefinitely until terminated with a stop command asserted by the control inputs.

Figure 11-19 to Figure 11-21 illustrate operation sequences after LOS detection.

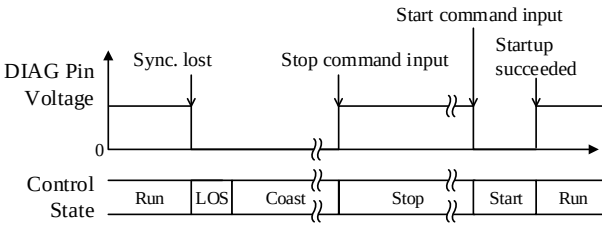


Figure 11-19. Restart by Command Input (RSC = 0, ESF = 1, DIAG[4:0] = 1)

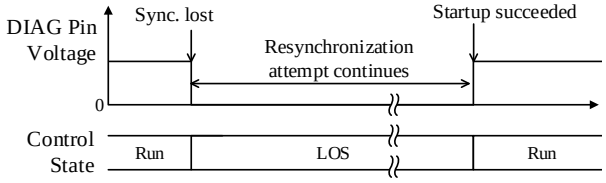


Figure 11-20. Restart by Sustained LOS Operation (RSC = 1 or 0, ESF = 0, DIAG[4:0] = 1)

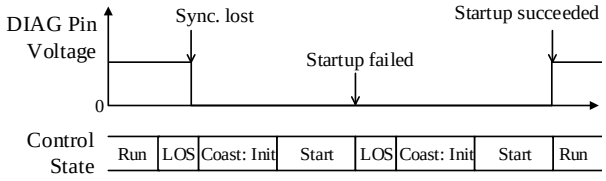


Figure 11-21. Restart by Auto-restart Sequence (RSC = 1, ESF = 1, DIAG[4:0] = 1)

11.16. Serial Communications

The IC has access to the internal registers through the serial communications, which uses two bus lines, SCL and SDA. Through these data lines, data is exchanged between the microcontroller as a master device and the IC as a subordinate device. The SCL (input) clock is generated in the master device. The SCL and SDA lines have a hysteresis-based glitch suppression circuit to enhance their noise immunities. The control sequences of communications are consist of the several steps listed below:

● Start Condition

A start condition is defined by a falling edge of the SDA line while the SCL line is high. The master device always initiates a start condition.

A start condition is permitted to occur at any time timing during a data transfer. The IC always responds the occurred start condition by resetting the data transfer sequence with ignoring all data from any incomplete register write.

● Address Cycle

An address cycle consists of the 7-bit register address, the R/W bit, and the acknowledge bit (see Figure 11-23) as follows:

- Register Address: 7 Bits

The 7-bit address. The first 2 bits, A[6:5], must be set to 0. The remaining 5 bits, A[4:0], select the register address for the first register access. The address is transferred MSB first.

- R/W Bit: 1 Bit (Read = 1, Write = 0)

The R/W bit defines the direction of data transfer. When R/W = 1, the master device reads one or more bytes from the IC. When R/W = 0, the master device writes one or more bytes to the IC. The register is updated only when two complete bytes are received.

- Acknowledge Bit: 1 Bit

The master device uses an acknowledge bit to check if the subordinate is responding to the address and data.

● Data Cycle

The 8-bit data following an acknowledge bit. A single register transfer requires 2 data cycles. The data is transferred MSB first.

● Stop Condition

A stop condition is defined by a rising edge of the SCL line while the SDA line is high.

Except for when indicating a start/stop condition, the master device must hold the SDA line to be low or high while the master device clock is high. The SDA line can be changed only when the SCL line is low.

When performing a write, the master device releases the SDA line to receive the acknowledgement during the 9th clock cycle following each data byte. After 2-byte data is received, the data is transferred to the register in the IC.

When reading the data from the IC, the master device acknowledges the address in the same manner as the write sequence. While the IC transmits the data to the master device, the master device holds the SDA line release state. The data transmission of the first 8 bits are completed, the master device puts the SDA line to low before the 9th clock cycle so that the master device can acknowledge the data. When the IC detects that the SDA line is low during the 9th clock cycle, the IC responds by transmitting the 2nd data byte to the master device. Then, the data byte is transmitted in pairs to the master device until the master device puts the SDA line to low. When the IC detects that the SDA line becomes low, the IC stops the data transfer and waits for a stop condition signal.

At power-on, when the V3 pin voltage increases to the V3 Pin UVP Threshold Voltage, V_{3UV} or more, the IC responds to the data transfer sequence. When the V3 pin voltage is less than V_{3UV}, the IC never respond to any request for the serial communications.

When writing to an arbitrary register, the IC ignores the first 6 bits, D[15:10].

When a read from an arbitrary register takes place, the first 6 bits contain the critical fault flags (i.e., same as the higher 6 bits in the Register 30). The remaining 10 bits, D[9:0], are the contents of the register address at that moment (except for the Register 28 and 30). When a read from the Register 28 takes place, the 10 bits, NVC[9:0], which follow the critical fault flags are the contents of the EEPROM write cycle counter. When reading the Register 30, the 7 bits which follow the critical fault flags are fault flags, including TW, OT, LOS, PMF, HOC, OVM, UVM. The remaining 3 bits are 0.

Figure 11-22 to Figure 11-27 are examples of the serial communications sequences.

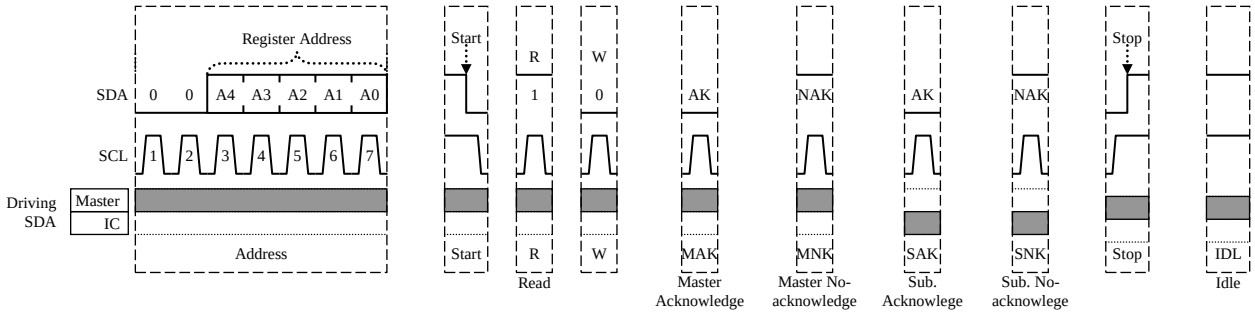


Figure 11-22. Serial Communications Sequence

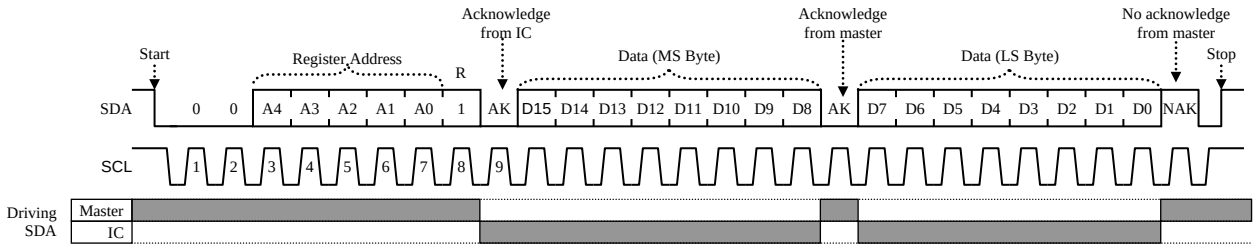


Figure 11-23. Single Word Read from Register

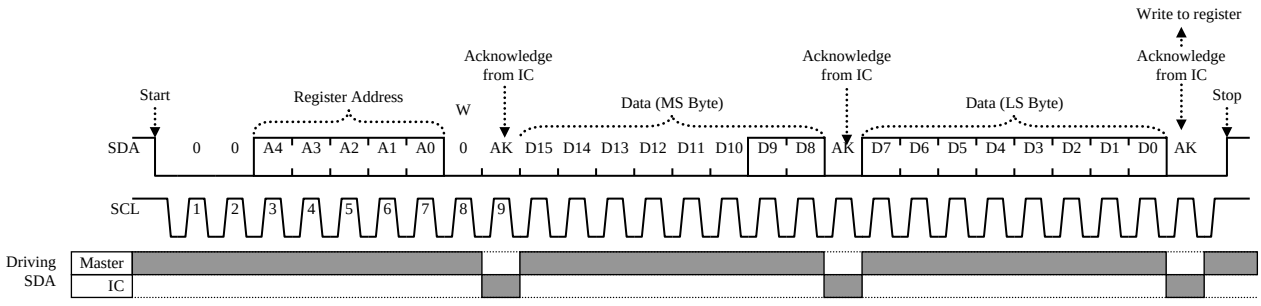


Figure 11-24. Single Word Write to Register

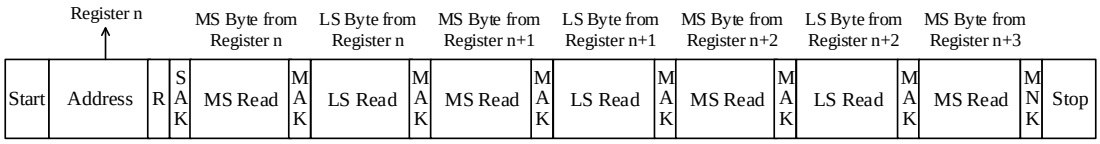


Figure 11-25. Multiple Reads from Register

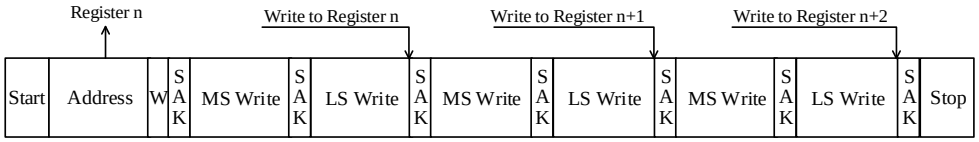


Figure 11-26. Multiple Writes to Register

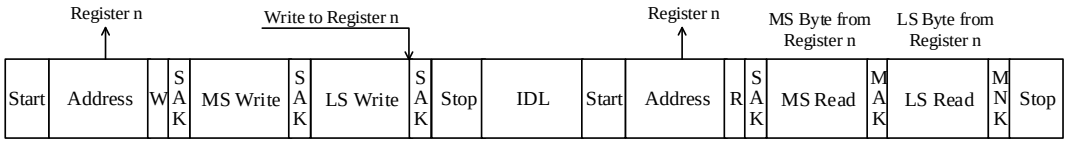


Figure 11-27. Write then Read Register

11.17. EEPROM

The IC integrates a non-volatile memory (EEPROM) which stores register data, thus enabling password-protected security.

11.17.1. Register Data Saving

The parameter settings are written to the EEPROM by setting the SAV bit in the Register 28 from "1" to "0". The register settings are read from the EEPROM after a power-on reset.

All the register settings are read from/written to the EEPROM as a single operation. Writing to/reading from the values of only a single register is not permitted.

Writing (saving data) to the EEPROM requires the EEPROM Write Supply Voltage, V_{PP}, to be applied to the VPP pin. For a stable voltage supply to the EEPROM, V_{PP} stepped down by the internal linear regulator is applied to the EEPROM.

Before a save sequence proceeds, V_{PP} must be applied within a specified period of time, t_{PRS}, and be continuously applied until the sequence completes. When no data save to the EEPROM is needed, the VPP pin may be left applied from V_{PP}, connected to the ground, or left open.

When the motor is still running at the time the save sequence proceeds, the IC turns off the power MOSFETs and enters the coast mode to stop the motor run. At this time, the IC ignores the inputs to the VSP pin and the motor control commands entered through the serial communications. Any changes occurred during the save sequence may or may not be written to the EEPROM. Reading from the Register 28 is the only recommended serial communications operation during the save sequence. The save sequence takes 700 ms (typ.) to complete.

When the save sequence completes successfully, the write count stored to the NVC[9:0] bits in the Register 28 is incremented and all the fault flag bits are cleared. An increment in the value of the NVC[9:0] bits indicates a successful save sequence completion; therefore, it is necessary to read the NVC value in the Register 28 before and after the save sequence.

The higher 6 bits in the Register 28 contain the critical fault flags. When the save sequence fails and a fault condition occurs, the FF bit is set to "1" to indicate a critical fault flag.

For data retention reliability, the guaranteed number of EEPROM writes should be set to less than 1000 times. When the EEPROM write cycle counter exceeds 1023, the EE bit in the diagnostic register (Register 30) is permanently set to "1", indicating the EEPROM overwrite fault flag. The write cycle counter then resets the existing count and continues counting from 0 to 1023. Once the EE bit is set to "1", the write cycle counter stops when reaching 1023. Note that the EE bit does not affect the states of the DIAG pin fault signal output or the FF bit in the diagnostic register.

11.17.2. Locking by Password

To protect the EEPROM from an overwrite or read operation, enable the password setting with the PWD[9:0] bits in the configuration register 11 (Config 11). Setting the PWD[9:0] bits to an arbitrary number other than 0 protects the EEPROM from any unauthorized access. When the PWD[9:0] bits are initially passed, the IC is capable of reading the EEPROM contents via the serial communications and of saving the configuration register contents to the EEPROM.

When the PWD[9:0] bits are set to 0, the IC is put into a password-unlocked state and thus becomes capable of reading from/writing to the configuration register contents (i.e., unlocked mode). In the unlocked mode, the IC performs the motor speed control with both of the VSP pin voltage and the configuration register contents.

When the PWD[9:0] bits are set to an arbitrary number other than 0 (but within the specified range), the IC enters a password-locked state, i.e., locked mode, immediately after a power-on reset or a return from the low power consumption mode. In the locked mode, reading from the EEPROM via the serial communications results in the state that IC outputs random numbers, except for the Registers 28, 30, and the PN[3:0] bits in the Config 15. The IC also performs the motor speed control with the VSP pin voltage only, according to the parameter settings previously stored in the EEPROM. In this operation, the IC ignores any changes to the configuration register contents.

- **Locking Procedure**

To enable the locked mode, follow the procedure below:

- Apply 15 V to the VCCx pin and 24 V to the VPP pin.
- Enter a password to the PWD[9:0] bits.
- Set the SAV bit from "1" to "0" in order to save the password to the EEPROM.
- Power off the VCCx and VPP pin voltages. The IC then operates in the locked mode.

- **Unlocking Procedure**

To release the locked mode, follow the procedure below:

- Apply 15 V to the VCCx pin and 24 V to the VPP pin.
- Enter the password to the PWD[9:0] bits, and wait for 15 seconds to clear the password.
- Power off the VCCx and VPP pin voltages. The IC then operates in the unlocked mode.

Table 11-8. Protection Mode Definitions

Function	Locked Mode	Unlocked Mode
Serial Write	Disabled(1)	Enabled
Serial Read	Random number output(2)	Enabled
Password: PWD[9:0]	Write only	Read/Write
ID Number: PN[3:0]	Read only	Read/Write
Register 30 (Diagnostic)	Read only	Read only
Register 29 (EEPROM)	Read only	Read only
Speed Control	VSP	VSP/Serial communications

(1) Except for the PWD[9:0] bits.
(2) Except for the PN[3:0] bits in the Config 15, and the Registers 28, 30.

11.18. Register Overview

The order of serial data transfer is MSB first in units of 16 bits. The first 5 bits are assigned as register addresses. The IC employs the registers consisting of:

- 22 system configuration registers
- 1 EEPROM setting register
- 2 diagnostic registers
- 1 motor operation setting register

The registers are grouped by their functions, as amply described in Section 11.20:

- **System Configuration Registers**
  Config 0: PWM Frequency
  Config 1: Basic Timing
  Config 2: Detection Timing
  Config 3: HOCP Detection Timing

- **Startup Setting Registers**
  Config 4: Startup Hold
  Config 5: Startup Timing

- **Motor Control Setting Registers**
  Config 6: Rotation Limitation
  Config 7: Current Limitation
  Config 8: Speed Control Gains, K_I
  Config 9: Current Control Gains, K_{CP} and K_{CI}
  Config 10: Phase Angle Control Gains, K_{TP} and K_{TI}
  Config 11: EEPROM Security Password
  Config 12: Motor Coil Inductance Multiplier
  Config 13: Magnetic Field Control
  Config 14: Dead Time Compensation

- **Speed Setting Register**
  Config 15: Speed Limitation
  Config 16: Speed Reference
  Config 17: Minimum Reference Speed
  Config 18: Maximum Speed Voltage
  Config 19: Excitation Start Voltage
  Config 20: Minimum Speed Voltage
  Config 21: Low Power Consumption Mode Transition Voltage

- **Internal Control Setting Registers**
  Register 28: EEPROM Control
  Register 29: Diagnostic Register Fault Mask
  Register 30: Diagnostic Register
  Register 31: Run Register

11.19. Register Map

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0	0	0	0	0	0	0	CR1	CR0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
Config 1	0	0	0	0	0	0	DT5	DT4	DT3	DT2	DT1	DT0	OHT3	OHT2	OHT1	OHT0
Config 2	0	0	0	0	0	0	CMS1	CMS0	RSN1	RSN0	OCF1	OCF0	CD3	CD2	CD1	CD0
Config 3	0	0	0	0	0	0	MO3	MO2	MO1	MO0	BCG2	BCG1	BCG0	IWM1	IWM0	IHO
Config 4	0	0	0	0	0	0	HT5	HT4	HT3	HT2	HT1	HT0	HD3	HD2	HD1	HD0
Config 5	0	0	0	0	0	0	STS4	STS3	STS2	STS1	STS0	STD4	STD3	STD2	STD1	STD0
Config 6	0	0	0	0	0	0	LS5	LS4	LS3	LS2	LS1	LS0	HS3	HS2	HS1	HS0
Config 7	0	0	0	0	0	0	IM4	IM3	IM2	IM1	IM0	IO4	IO3	IO2	IO1	IO0
Config 8	0	0	0	0	0	0	UVS	HR3	HR2	HR1	HR0	FGS	SI3	SI2	SI1	SI0
Config 9	0	0	0	0	0	0	0	CP3	CP2	CP1	CP0	ETR	CI3	CI2	CI1	CI0
Config 10	0	0	0	0	0	0	—	TP3	TP2	TP1	TP0	—	TI3	TI2	TI1	TI0
Config 11	0	0	0	0	0	0	PWD9	PWD8	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
Config 12	0	0	0	0	0	0	LW9	LW8	LW7	LW6	LW5	LW4	LW3	LW2	LW1	LW0
Config 13	0	0	0	0	0	0	XWM1	XWM0	LHT1	LHT0	FW5	FW4	FW3	FW2	FW1	FW0
Config 14	0	0	0	0	0	0	DTC	—	DG3	DG2	DG1	DG0	DM3	DM2	DM1	DM0
Config 15	0	0	0	0	0	0	SCS	—	PN3	PN2	PN1	PN0	SU3	SU2	SU1	SU0
Config 16	0	0	0	0	0	0	SR9 SRH9	SR8 SRH8	SR7 SRH7	SR6 SRH6	SR5 SRH5	SR4 SRH4	SR3 SRH3	SR2 SRH2	SR1 SRH1	SR0 SRH0
Config 17	0	0	0	0	0	0	SRL9	SRL8	SRL7	SRL6	SRL5	SRL4	SRL3	SRL2	SRL1	SRL0
Config 18	0	0	0	0	0	0	VX9	VX8	VX7	VX6	VX5	VX4	VX3	VX2	VX1	VX0
Config 19	0	0	0	0	0	0	VS9	VS8	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
Config 20	0	0	0	0	0	0	VN9	VN8	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0
Config 21	0	0	0	0	0	0	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Register 28 Write EEPROM Control	0	0	0	0	0	0	SAV	—	—	—	—	—	—	—	—	—
Register 28 Read EEPROM Count	0	0	0	0	0	0	NVC9	NVC8	NVC7	NVC6	NVC5	NVC4	NVC3	NVC2	NVC1	NVC0
Register 29 Fault Mask	0	0	0	0	0	0	TW	OT	LOS	PMF	HOC	OVM	UVM	—	—	—
Register 30 Write	0	0	0	0	0	0	—	—	—	—	—	DIAG4	DIAG3	DIAG2	—	—
Register 30 Read Diagnostic	FF	POR	ME	WD	OC	EE	TW	OT	LOS	PMF	HOC	OVM	UVM	—	—	—
Register 31 Run	0	0	0	0	0	0	DIAG1	DIAG0	RDG	PMR	STM	ESF	RSC	BRK	DIR	RUN
Register Read	FF	POR	ME	WD	OC	EE										

11.20. Configuration Registers

This section describes the register contents. The checkmark in the Ref. column indicates the row that contains the reference register values (i.e., the parameters that the GUI initially displays) tabulated in Section 5.

11.20.1. System Configuration Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 0	0	0	0	0	0	0	CR1	CR0	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
Config 1	0	0	0	0	0	0	DT5	DT4	DT3	DT2	DT1	DT0	OHT3	OHT2	OHT1	OHT0

Config 0: PWM Frequency

CR[1:0]

The CR[1:0] bits are for setting the maximum input range of the current-sensing operational amplifiers. For more details, see Section 11.13.

CR1	CR0	Maximum Input Range	Ref.
0	0	−500 mV to 500 mV	✓
0	1	−250 mV to 250 mV	
1	0	−125 mV to 125 mV	
1	1	−62.5 mV to 62.5 mV	

PR[7:0]

The PR[7:0] bits are for setting a PWM period, T_{PR}, used for the PWM current control for motor control system. For more details on the PWM control, see Section 11.9.

The equation below defines T_{PR}, which should range from 30.5 µs to 132.5 µs:

$$T_{PR}\ (\mu s) = 30.5 + (n \times 0.4)\ . \qquad (16)$$

Where n is a positive integer determined by the PR[7:0] bits. For example, when PR[7:0] = [0100 0111], T_{PR} = 58.9 µs.

Config 1: Basic Timing

DT[5:0]

The DT[5:0] bits are for setting a dead time, t_{DEAD}. Be sure to set the t_{DEAD} so that it falls within the recommended operating range (i.e., ≥1.5 µs).

The equation below defines t_{DEAD}, which should range from 100 ns to 3.15 µs in increments of 50 ns:

$$t_{DEAD} = n \times 50\ ns\ . \qquad (17)$$

Where n is a positive integer determined by the DT[5:0] bits. A minimal value of t_{DEAD} is 100 ns. For example, when DT[5:0] = [01 1110], t_{DEAD} = 1.5 µs.

OHT[3:0]

The OHT[3:0] bits are for setting a hold time of the hard overcurrent protection, t_{HOC}. For more details on the HOCP function, see Section 11.15.7.

The equation below defines t_{HOC}, which should range from 100 ms to 1.6 s in increments of 100 ms:

$$t_{HOC} = (1 + n) \times 100\ ms\ . \qquad (18)$$

Where n is a positive integer determined by the OHT[3:0] bits. For example, when OHT[3:0] = [1001], t_{HOC} = 1.0 s.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 2	0	0	0	0	0	0	CMS1	CMS0	RSN1	RSN0	OCF1	OCF0	CD3	CD2	CD1	CD0

Config 2: Detection Timing

CMS[1:0]

Select the PWM switching mode to be enabled by setting the CMS[1:0] bits as defined below. For more details on the PWM switching modes, see Section 11.11.

CMS1	CMS0	PWM Switching Mode	Ref.
0	0	2-phase PWM switching	
0	1	3-phase PWM switching	
1	0	Prohibited	
1	1	Automatically shifts between 2-/3-phase PWM switching modes - Shifts from 3-phase to 2-phase PWM switching at a modulation index of ≥50% - Shifts from 2-phase to 3-phase PWM switching at a modulation index of <25%	✓

RSN[1:0]

Select the number of restarts allowed after a startup failure by setting the RSN[1:0] bits as defined below.

RSN1	RSN0	Number of Restarts Allowed	Ref.
0	0	5 times	
0	1	10 times	✓
1	0	20 times	
1	1	Infinite	

OCF[1:0]

Select an HOCP filtering time, t_{OCF}, by setting the OCF[1:0] bits as defined below. For more details on the HOCP function, see Section 11.15.7.

OCF1	OCF0	Filtering Time, t_{OCF}	Ref.
0	0	2.0 µs	
0	1	1.5 µs	
1	0	1.0 µs	✓
1	1	0.5 µs	

CD[3:0]

The CD[3:0] bits are for setting a current detection delay time, t_{CD}, which starts later than the midpoint of a predetermined PWM period. For more details, see Section 11.13. The equation below defines t_{CD}, which should range from 0 µs to 3 µs:

$$t_{CD} = n \times 200\ \text{ns}\ . \quad (19)$$

Where n is a positive integer determined by the CD[3:0] bits. For example, when CD[3:0] = [0011], t_{CD} = 0.6 µs.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 3	0	0	0	0	0	0	MO3	MO2	MO1	MO0	BCG2	BCG1	BCG0	IWM1	IWM0	IHO

Config 3: HOCP Detection Timing

MO[3:0]

The MO[3:0] bits are for setting a minimum on-time, t_{MO}, for current detection. The equation below defines t_{MO}, which should range from 0 µs to 6 µs:

$$t_{MO} = n \times 400\ \text{ns}. \quad (20)$$

Where n is a positive integer determined by the MO[3:0] bits. For example, when MO[3:0] = [0101], t_{MO} = 2.0 µs.

BCG[2:0]

Select a charging time of bootstrap capacitor, t_{BCG}, by setting the BCG[2:0] bits as defined below. For more details, see Section 11.12.

BCG2	BCG1	BCG0	Charging Time, t_{BCG}	Ref.
0	0	0	No bootstrap charging	
0	0	1	1 ms	
0	1	0	2 ms	
0	1	1	5 ms	
1	0	0	10 ms	✓
1	0	1	20 ms	
1	1	0	50 ms	
1	1	1	100 ms	

IWM[1:0]

Select a windmill braking current, I_{WM}, by setting the IWM[1:0] bits as defined below. I_{MX} represents a maximum operating current.

IWM1	IWM0	Windmill Braking Current, I_{WM}	Ref.
0	0	25% I_{MX}	✓
0	1	50% I_{MX}	
1	0	75% I_{MX}	
1	1	100% I_{MX}	

IHO

The IHO bit is for setting an HOCP threshold current, I_{HOC}. Select either 150% or 200% of the maximum current detection range, I_{FS}, by setting the IHO bit as defined below.

IHO	HOCP Threshold Current	Ref.
0	150% I_{FS}	✓
1	200% I_{FS}	

11.20.2. Startup Setting Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 4	0	0	0	0	0	0	HT5	HT4	HT3	HT2	HT1	HT0	HD3	HD2	HD1	HD0
Config 5	0	0	0	0	0	0	STS4	STS3	STS2	STS1	STS0	STD4	STD3	STD2	STD1	STD0

Config 4: Startup Hold

HT[5:0]

The HT [5:0] bits are for setting a startup hold time, t_{HOLD}. The following equations define t_{HOLD} according to a PWM period, T_{PR}, determined by the PR[7:0] bits.

- **When T_{PR} = 125.3 µs to 132.5 µs:**

$$t_{HOLD} = T_{PR} \times n \times 400 \text{ ms} . \quad (21)$$

- **When T_{PR} = 62.5 µs to 124.9 µs:**

$$t_{HOLD} = T_{PR} \times n \times 800 \text{ ms} . \quad (22)$$

- **When T_{PR} = 41.7 µs to 62.1 µs:**

$$t_{HOLD} = T_{PR} \times n \times 1200 \text{ ms} . \quad (23)$$

- **When T_{PR} = 30.5 µs to 41.3 µs:**

$$t_{HOLD} = T_{PR} \times n \times 1600 \text{ ms} . \quad (24)$$

Where n is a positive integer determined by the HT[5:0] bits. For example, when PR[7:0] = [0100 0111] and HT[5:0] = [00 0101], T_{PR} = 58.9 µs as calculated by Equation (16). Thus, t_{HOLD} = 353.4 ms based on Equation (22).

HD[3:0]

The HD[3:0] bits are for setting the duty cycle of a startup hold current, D_{HOLD}. The equation below defines D_{HOLD} with the maximum current detection range, I_{FS}. D_{HOLD} should range from 0% to 22.89%.

$$D_{HOLD} = n \times 1.525\% . \quad (25)$$

Where n is a positive integer determined by the HD[3:0] bits. For example, when HD[3:0] = [0100], D_{HOLD} = 6.1%.

Config 5: Startup Timing

STS[4:0]

The STS[4:0] bits are for setting a driving frequency at startup, f_{ST}. The equation below defines f_{ST}, which should range from 0 Hz to 49.6 Hz:

$$f_{ST} = n \times 1.6 \text{ Hz} . \quad (26)$$

Where n is a positive integer determined by the STS[4:0] bits. For example, when STS[4:0] = [0 1000], f_{ST} = 12.8 Hz.

STD[4:0]

The STD[4:0] bits are for setting parameters for the two startup modes: a duty cycle at startup, D_{ST}, for the DC alignment start mode; a driving current, I_{RAMP}, for the ramp-up start mode.

The equation below defines D_{ST}, which should range from 0% to 48.44%:

$$D_{ST} = n \times 1.5625\% . \quad (27)$$

Where n is a positive integer determined by the STD[4:0] bits. For example, when STD[4:0] = [0 0100], D_{ST} = 6.3%.

The equation below defines I_{RAMP}, which should range from 0% I_{FS} to 48.44% I_{FS}:

$$I_{RAMP} = n \times 1.5625\% \times I_{FS} . \quad (28)$$

Where n is a positive integer determined by the STD[4:0] bits. For example, when STD[4:0] = [0 0100], I_{RAMP} = 6.3% I_{FS}.

11.20.3. Motor Control Setting Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 6	0	0	0	0	0	0	LS5	LS4	LS3	LS2	LS1	LS0	HS3	HS2	HS1	HS0
Config 7	0	0	0	0	0	0	IM4	IM3	IM2	IM1	IM0	IO4	IO3	IO2	IO1	IO0

Config 6: Rotation Limitation

Section 11.15.10 explains the loss-of-synchronization protection in detail.

LS[5:0]

The LS[5:0] bits are for setting a lowest speed threshold, f_{LS}. The equation below defines f_{LS}, which should range from 0 Hz to 50.4 Hz. When f_{LS} = 0, the lowest speed detection is disabled.

$$f_{LS} = n \times 0.8\ \text{Hz}\,. \quad (29)$$

Where n is a positive integer determined by the LS[5:0] bits. For example, when LS[5:0] = [00 0000], f_{LS} = 0 Hz.

HS[3:0]

The HS[3:0] bits are for setting a highest speed threshold, f_{HS}. The equation below defines f_{HS}, which should range from 0 Hz to 1536 Hz. When f_{HS} = 0, the highest speed detection is disabled.

$$f_{HS} = n \times 102.4\ \text{Hz}\,. \quad (30)$$

Where n is a positive integer determined by the HS[3:0] bits. For example, when HS[3:0] = [0101], f_{HS} = 512 Hz.

Config 7: Current Limitation

IM[4:0]

The IM[4:0] bits are for setting a maximum operating current, I_{MX}. For more details, see Section 11.13.

The equation below defines I_{MX} with the maximum current detection range, I_{FS}. I_{MX} should range from 38% I_{FS} to 100% I_{FS}.

$$I_{MX} = [38 + (n \times 2)](\%) \times I_{FS}\,. \quad (31)$$

Where n is a positive integer determined by the IM[4:0] bits. For example, when IM[4:0] = [0 0110], I_{MX} = 50% IFS.

IO[4:0]

The IO[4:0] bits are for setting an SOCP threshold current, I_{LIM}. When IO[4:0] = 0, the SOCP function is disabled. For more details, see Section 11.15.6.

The equation below defines I_{LIM} with the maximum current detection range, I_{FS}. I_{LIM} should range from 38% I_{FS} to 100% I_{FS}.

$$I_{LIM} = [38 + (n \times 2)](\%) \times I_{FS}\,. \quad (32)$$

Where n is a positive integer determined by the IO[4:0] bits. For example, when IO[4:0] = [1 0101], I_{LIM} = 80% I_{FS}.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 8	0	0	0	0	0	0	UVS	HR3	HR2	HR1	HR0	FGS	SI3	SI2	SI1	SI0

Config 8: Speed Control Gains, K_I

UVS

The UVS bit is for setting a motor undervoltage threshold, V_{UM} (i.e., the VM pin threshold voltage used for detecting a voltage drop in V_{DC}; see Section 11.15.4). Select either a 0.3 V or 0.6 V threshold voltage by setting the UVS bit as defined below.

UVS	VM Pin UVP Threshold Voltage	Ref.
0	0.3 V	✓ 4
1	0.6 V	

HR[3:0]

The HR[3:0] bits are for setting a ramp-up time of the hold current, t_{HRMP}.

The equation below defines t_{HRMP}, which should range from 0% t_{HOLD} to 93.75% t_{HOLD}:

$$t_{HRMP} = (n \times 6.25)\ (\%) \times t_{HOLD}\ . \quad (33)$$

Where n is a positive integer determined by the HR[3:0] bits. For example, when HR[3:0] = [1000], t_{HRMP} = 50% t_{HOLD}.

FGS

The FGS bit is for setting an output pulse frequency of the FG pin. Select either a ×1 or ×3 motor electrical cycle frequency by setting the FGS bit as defined below.

FGS	FG Pin Output Pulse Frequency	Ref.
0	Motor electrical cycle frequency: ×1	✓
1	Motor electrical cycle frequency: ×3	

SI[3:0]

The SI[3:0] bits are for setting a constant of the integral gain constant, K_I, used for the speed control. The equation below defines K_I, which should range from 1/128 K_{NSI} to 256 K_{NSI}:

$$K_I = 2^{(n-7)} \times K_{NSI}\ . \quad (34)$$

Where n is a positive integer determined by the SI[3:0] bits, and K_{NSI} is a fixed integral gain of the speed control.

For example, when SI[3:0] = [0110], K_{SI} = 0.5 K_{NSI}.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 9	0	0	0	0	0	0	0	CP3	CP2	CP1	CP0	ETR	CI3	CI2	CI1	CI0
Config 10	0	0	0	0	0	0	—	TP3	TP2	TP1	TP0	—	TI3	TI2	TI1	TI0

Config 9: Current Control Gains, K_{CP} and K_{CI}

CP[3:0]

The CP[3:0] bits are for setting a constant of the proportional gain, K_{CP}, used for the current control. The equation below defines K_{CP}, which should range from 1/128 K_{NCP} to 256 K_{NCP}:

$$K_{CP} = 2^{(n-7)} \times K_{NCP} . \quad (35)$$

Where n is a positive integer determined by the CP[3:0] bits, and K_{NSI} is a fixed proportional gain of the current control.

For example, when CP[3:0] = [0110], K_{CP} = 0.5 K_{NCP}.

ETR

The ETR bit is for setting a ramp-up current for motor restart.

ETR	Ramp-up Current Setting	Ref.
0	Restart with fixed ramp-up current	✓
1	Restart with spread ramp-up current	

CI[3:0]

The CI[3:0] bits are for setting a constant of the integral gain, K_{CI}, used for the current control. The equation below defines K_{CI}, which should range from 1/128 K_{NCI} to 256 K_{NCI}:

$$K_{CI} = 2^{(n-7)} \times K_{NCI} . \quad (36)$$

Where n is a positive integer determined by the CI[3:0] bits, and K_{NCI} is a fixed integral gain of the current control.

For example, when CI[3:0] = [0110], K_{CI} = 0.5 K_{NCI}.

Config 10: Phase Angle Control Gains, K_{TP} and K_{TI}

TP[3:0]

The TP[3:0] bits are for setting a constant of the proportional gain, K_{TP}, used for phase angle control. The equation below defines K_{TP}, which should range from 1/128 KNTP to 256 K_{NTP}:

$$K_{TP} = 2^{(n-7)} \times K_{NTP} . \quad (37)$$

Where n is a positive integer determined by the TP[3:0] bits, and K_{NTP} is a fixed proportional gain of the sensorless control.

For example, when TP[3:0] = [0110], K_{TP} = 0.5 K_{NTP}.

TI[3:0]

The TI[3:0] bits are for setting a constant of the integral gain, K_{TI}, used for phase angle control. The equation below defines K_{TI}, which should range from 1/128 K_{NTI} to 256 K_{NTI}:

$$K_{TI} = 2^{(n-7)} \times K_{NTI} . \quad (38)$$

Where n is a positive integer determined by the TI[3:0] bits, and K_{NTI} is an integral gain of the sensorless control.

For example, when TI[3:0] = [0110], K_{TI} = 0.5 K_{NTI}.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 11	0	0	0	0	0	0	PWD9	PWD8	PWD7	PWD6	PWD5	PWD4	PWD3	PWD2	PWD1	PWD0
Config 12	0	0	0	0	0	0	LW9	LW8	LW7	LW6	LW5	LW4	LW3	LW2	LW1	LW0

Config 11: EEPROM Security Password

PWD[9:0]

The PWD[9:0] bits are for setting a password for controlling access to the EEPROM. The setting range is from 0 to 1023. For more details, see Section 11.17.2.

Config 12: Motor Coil Inductance Multiplier

LW[9:0]

The LW[9:0] bits are for setting an inductance of the motor winding, L_{WM}. The equation below defines L_{WM}, which should range from 0 L_U to 1023 L_U:

$$L_{WM} = n \times L_U \, . \tag{39}$$

Where n is a positive integer determined by the LW[9:0] bits, and L_U is a factor of the inductance.

For example, when LW[9:0] = [00 1100 1000], L_{WM} = 200 L_U.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 13	0	0	0	0	0	0	XWM1	XWM0	LHT1	LHT0	FW5	FW4	FW3	FW2	FW1	FW0
Config 14	0	0	0	0	0	0	DTC	—	DG3	DG2	DG1	DG0	DM3	DM2	DM1	DM0

Config 13: Magnetic Field Control

XWM[1:0]

Select a minimum threshold of the windmill braking current by setting the XWM[1:0] bits as defined below. I_{MX} represents a maximum operating current. When the braking current falls below this minimum threshold, the IC considers motor operations to be stopped (see Section 11.5).

XWM1	XWM0	Minimum Braking Current Threshold	Ref.
0	0	6.25% I_{MX}	✓
0	1	12.50% I_{MX}	
1	0	18.75% I_{MX}	
1	1	25.00% I_{MX}	

LHT[1:0]

The LHT[1:0] bits are for setting a hold time after an LOS (loss of synchronization) fault occurs.

LHT1	LHT0	LOS Fault Hold Time	Ref.
0	0	800 ms	✓
0	1	400 ms	
1	0	200 ms	
1	1	100 ms	

FW[5:0]

The FW[5:0] bits are for setting a field weakening current, I_{FW}. When $I_{FW} < 0$, the motor operates in field enhancement mode; when $I_{FW} > 0$, the motor operates in field weakening mode.

The equation below defines I_{FW} with the maximum current detection range, I_{FS}. I_{FW} should range from −26% I_{FS} to 100% I_{FS}.

$$I_{FW} = (n - 13) \times 2(\%) \times I_{FS} . \quad (40)$$

Where n is a positive integer determined by the FW[5:0] bits.

For example, when FW[5:0] = [00 1101], I_{FW} = 0% I_{FS}.

Config 14: Dead Time Compensation

DTC

The DTC bit enables or disables the dead time compensation.

DTC	Dead Time Compensation	Ref.
0	Disabled	✓
1	Enabled	

VMC

The VMC bit enables or disables the compensation of the VM pin voltage.

VMC	VM Pin Voltage Compensation	Ref.
0	Disabled	
1	Enabled	✓

DG[3:0]

The DG[3:0] bits are for setting a dead time compensation gain, K_{DTC}. The equation below defines K_{DTC}, which should range from 0 to 15:

$$K_{DTC} = n . \quad (41)$$

Where n is a positive integer determined by the DG[3:0] bits.

DM[3:0]

The DM[3:0] bits are for setting a compensation ratio of the maximum dead time, t_{DCM} (%).The equation below defines t_{DCM} with the dead time, t_{DEAD}. t_{DCM} should range from 0% to 93.75%.

$$t_{DCM} = n \times 6.25\ (\%)\ t_{DEAD} . \quad (42)$$

Where n is a positive integer determined by the DM[3:0] bits.

11.20.4. Speed Setting Registers

For the motor speed setting, see Section 11.7.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 15	0	0	0	0	0	0	SCS	—	PN3	PN2	PN1	PN0	SU3	SU2	SU1	SU0
Config 16	0	0	0	0	0	0	SR9 SRH9	SR8 SRH8	SR7 SRH7	SR6 SRH6	SR5 SRH5	SR4 SRH4	SR3 SRH3	SR2 SRH2	SR1 SRH1	SR0 SRH0

Config 15: Speed Limitation

SCS

Select the speed control mode to be enabled by setting the SCS bit as defined below.

SCS	Speed Control Mode	Ref.
0	Controlled by externally input voltage on the VSP pin (external mode)	
1	Controlled by internal register settings	✓

PN[3:0]

The PN[3:0] bits constitute a user-assigned variable used as an identification number or a revision number. The setting range is from 0 to 15.

SU[3:0]

The SU[3:0] bits are for setting a multiplier, f_U, of the reference speed, f_{REF}. The equation below defines f_U, which should range from 0 Hz to 1.6 Hz.

$$f_U = (1 + n) \times 0.1 \text{ (Hz)} . \quad (43)$$

Where n is a positive integer determined by the SU[3:0] bits. For example, when [3:0] = [1001], f_U = 1.0 Hz.

Config 16: Speed Reference

SR[9:0]

SRH[9:0]

- **SCS = 1**

When SCS = 1, the motor reference speed, f_{REF}, is set by the parameters directly input via the serial communications. In this option, the IC ignores the VSP pin input voltage and only uses the value in the SR[9:0] bits.

Hence, the SR[9:0] bits are for setting f_{REF}. The equation below defines f_{REF}, which should range from 0 f_U to 1023 f_U:

$$f_{REF} = n \times f_U \text{ (Hz)} . \quad (44)$$

Where n is a positive integer determined by the SR[9:0] bits, and f_U is a multiplier of the speed range. For example, when SR[9:0] = [00 0001 1110], fREF = 30 f_U.

The equation below calculates an actual motor speed, from the excitation frequency, f_{REF}, and the number of magnetic pole pairs in the motor, N_{PP}:

$$S = \frac{(f_{REF} \times 60)}{N_{PP}} . \quad (45)$$

When f_{REF} = 30 f_U, N_{PP} = 4, and f_U = 1.0 Hz, for instance, we will find the actual motor speed as follows:

$$S = \left(\frac{30 \times 1.0 \times 60}{4}\right) = 450 \text{ rpm} .$$

- **SCS = 0**

When SCS = 0, the IC uses the parameters in the SRH[9:0] bits to control the motor speed, not the SR[9:0] bits. In the external mode, the SRH[9:0] bits determine the maximum reference speed, f_{RH}, corresponding to the VSP pin input.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 17	0	0	0	0	0	0	SRL9	SRL8	SRL7	SRL6	SRL5	SRL4	SRL3	SRL2	SRL1	SRL0

Config 17: Minimum Reference Speed

SRL[9:0]

The SRL[9:0] bits are for setting the minimum reference speed, f_{RL}, which corresponds to the VSP pin input voltage. The equation below defines f_{RL}:

$$f_{RL} = n \times f_U \,. \tag{46}$$

Where n is a positive integer determined by the SRL[9:0] bits, and f_U is a multiplier of the speed range. For example, when SRL[9:0] = [00 0000 0000], $f_{RL} = 0\ f_U$.

The equation below calculates an actual minimum motor speed, from the minimum reference speed, f_{RL}, and the number of magnetic pole pairs in the motor, N_{PP}:

$$S_{MIN} = \frac{(f_{RL} \times 60)}{N_{PP}}. \tag{47}$$

When $f_{RL} = 0\ f_U$, NPP = 4, f_U = 1.0 Hz, for instance, we will find the actual minimum motor speed as follows:

$$S_{MIN} = \left(\frac{0 \times 1.0 \times 60}{4}\right) = 0 \text{ rpm}\,.$$

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config 18	0	0	0	0	0	0	VX9	VX8	VX7	VX6	VX5	VX4	VX3	VX2	VX1	VX0
Config 19	0	0	0	0	0	0	VS9	VS8	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
Config 20	0	0	0	0	0	0	VN9	VN8	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0
Config 21	0	0	0	0	0	0	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0

Config 18: Maximum Speed Voltage

VX[9:0]

The VX[9:0] bits are for setting the VSP pin voltage at which the motor reaches its maximum speed, V_{SMX}. The equation below defines V_{SMX}, which should range from 0 V to 5.88 V.

$$V_{SMX} = \frac{n}{174} \text{ (V)} . \quad (48)$$

Where n is a positive integer determined by the VX[9:0] bits. For example, when VX[9:0] = [11 0110 0110] at power-on reset, V_{SMX} = 5.000 V.

Config 19: Excitation Start Voltage

VS[9:0]

The VS[9:0] bits are for setting the VSP pin voltage at which the motor starts excitation, V_{SST}. The equation below defines V_{SST}, which should range from 0 V to 5.88 V.

$$V_{SST} = \frac{n}{174} \text{ (V)} . \quad (49)$$

Where n is a positive integer determined by the VS[9:0] bits. For example, when VS[9:0] = [01 1011 0011] at power-on reset, V_{SST} = 2.500 V.

Config 20: Minimum Speed Voltage

VN[9:0]

The VN[9:0] bits are for setting the VSP pin voltage at which the motor reaches its minimum speed, V_{SMN}. The equation below defines V_{SMN}, which should range from 0 V to 5.88 V.

$$V_{SMN} = \frac{n}{174} \text{ (V)} . \quad (50)$$

Where n is a positive integer determined by the VN[9:0] bits. For example, when VN[9:0] = [01 0101 1100] at power-on reset, V_{SMN} = 2.000 V.

Config 21: Low Power Consumption Mode Transition Voltage

VC[9:0]

The VC[9:0] bits are for setting the VSP pin voltage at which the IC enters the low power consumption mode, V_{SSN}. The equation below defines V_{SSN}, which should range from 0 V to 5.88 V.

$$V_{SSN} = \frac{n}{174} \text{ (V)} . \quad (51)$$

Where n is a positive integer determined by the VC[9:0] bits. For example, when VC[9:0] = [00 1010 1110] at power-on reset, V_{SSN} = 1.000 V.

11.20.5. Internal Control Setting Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 28 Write EEPROM Control	0	0	0	0	0	0	SAV	—	—	—	—	—	—	—	—	—
Register 28 Read EEPROM Count	0	0	0	0	0	0	NVC9	NVC8	NVC7	NVC6	NVC5	NVC4	NVC3	NVC2	NVC1	NVC0
Register 29 Fault Mask	0	0	0	0	0	0	TW	OT	LOS	PMF	HOC	OVM	UVM	—	—	—

Register 28: EEPROM Control

Section 11.17 provides further information.

- **Write**

SAV

When the SAV bit is changed from "1" to "0" in the case where the motor stops and the IC is in the unlocked mode, the following parameters are written to the EEPROM:

- Config 0 to Config 21
- Register 29 (Diagnostic Register Fault Mask)
- Register 31 (Run Register)

After the writing completes, the values of the NVC[9:0] bits are incremented by 1.

- **Read**

NVC[9:0]

The NVC[9:0] bits operate as EEPROM write counter outputs. After the writing to the EEPROM completes, the values of the NVC[9:0] bits are incremented by 1. When the number of write count exceeds 1023 times, the EE bit in the diagnostic register is permanently set to "1".

Register 29: Diagnostic Register Fault Mask

To disable each diagnostic function, set the corresponding bit to "1".

Bit Name	Fault Description
TW	Thermal warning
OT	Thermal shutdown
LOS	Loss of synchronization
PMF	Power module fault
HOC	Hard Overcurrent
OVM	VM pin overvoltage
UVM	VM pin undervoltage

	Fault Mask Setting for Diagnostic Register	Ref.
0	Diagnostic function enabled	✓
1	Diagnostic function disabled	

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 30 Write	0	0	0	0	0	0	—	—	—	—	—	DIAG4	DIAG3	DIAG2	—	—
Register 30 Read Diagnostic	FF	POR	ME	WD	OC	EE	TW	OT	LOS	PMF	HOC	OVM	UVM	—	—	—

Register 30: Diagnostic Register

● **Write**

Select which fault signals the DIAG pin will output by setting the DIAG[4:0] bits in Register 30 and Register 31. When a fault status is detected, the DIAG pin becomes logic low.

The table below lists the DIAG[4:0] bits settings.

DIAG[4:0]	DIAG Pin Fault Signal to Be Output	Ref.
0	General fault flag (FF)	✓
1	Loss of synchronization (LOS)	
2	Temperature output of control MIC	
3	Clock	
4	PWMDIR*	
5	SHTRIG*	
6	ADDONE*	
7	CLFLK_SYN*	
8	CLFLK_ASYN*	
9	PWM output (HIN1)	
10	PWM output (LIN1)	
11	PWM output (HIN2)	
12	PWM output (LIN2)	
13	PWM output (HIN3)	
14	PWM output (LIN3)	
15	Watchdog timeout	
16	Watchdog active	
17	Power module fault (PMF)	
18	Power module fault (PMF) reset	
19	Hard overcurrent (HOC)	
20	q-axis current	
21	—	
22	—	
23	—	
24 to 31	Reserved	

* Not used in motor designing.

● **Read**

When a fault status is detected, the corresponding bit is set to “1”. Section 11.14.2 explains the diagnostic register in detail; Section 11.15 provides detailed descriptions on the protections.

Bit Name	Fault Description
FF	General fault flag
POR	V3 pin undervoltage (power-on reset)
ME	Memory error
WD	Watchdog timeout
OC	Soft overcurrent
EE	EEPROM overwrite limit
TW	Thermal warning for control MIC
OT	Thermal shutdown for control MIC
LOS	Loss of synchronization
PMF	Power module fault (thermal shutdown for gate-drive MIC, low-side UVLO)
HOC	Hard overcurrent
OVM	VM pin overvoltage
UVM	VM pin undervoltage

	Fault Detection
0	No fault detected
1	Fault detected

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 31 Run	0	0	0	0	0	0	DIAG1	DIAG0	RDG	PMR	STM	ESF	RSC	BRK	DIR	RUN

Register 31: Run Register

For the DIAG[1:0] bits, see the Register 30 definition table.

RDG

The RDG bit determines whether to clear the DIAG pin status that the GUI displays. When RDG = 0, the controls related to the restart operations are disabled.

RDG	GUI Display Setting	Ref.
0	The fault status displayed on the GUI is cleared.	
1	The fault status displayed on the GUI is not cleared (latched).	✓

PMR

The PMR bit selects whether to put the gate-drive MIC into a standby state, in accordance with the reset operation by the RESETn pin.

PMR	Power Module Reset Selection	Ref.
0	The gate-drive MIC enters a standby state, according to the RESETn input signal.	✓
1	The gate-drive MIC does not enter a standby state.	

STM

The STM bit selects the startup mode.

STM	Startup Mode	Ref.
0	Ramp-up start mode	✓
1	DC alignment start mode	

ESF

The ESF bit selects the protective operation to be performed at fault detection (see Section 11.14.3).

ESF	Protective Operation	Ref.
0	The motor keeps driving; the corresponding fault flag in the diagnostic register is set.	
1	All the power MOSFETs turn off; the corresponding fault flag in the diagnostic register is set.	✓

RSC

The RSC bit selects whether to restart motor operations when a loss-of-synchronization (LOS) condition is detected (see Section 11.15.10).

RSC	Motor Restart Selection	Ref.
0	No restart (The motor stops with coasting upon LOS detection.)	✓
1	Restart allowed (The motor restarts upon LOS, SOCP, or HOCP detection when RSC = 1, RUN = 1, and BRK = 0.)	

BRK

The BRK bit controls braking operation. The braking operation is enabled only when RUN = 1. When RUN = 1 and BRK = 1, all the low-side power MOSFETs turn on to produce electrodynamic braking. Note that the BRK bit does not affect the braking operation in the startup sequence.

BRK	Braking Control	Ref.
0	Normal operation (brake off)	✓
1	Braking operation (brake on)	

DIR

The DIR bit is for setting the direction of motor rotation.

DIR Bit	DIR Pin	Motor Direction	DIR Bit Ref.
0	L	Forward	
0	H	Reverse	
1	L	Reverse	✓
1	H	Forward	✓

RUN

The RUN bit controls the start/stop operations of the motor.

RUN	Motor Start/Stop	Ref.
0	Excitation stops	✓
1	Motor run starts	

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Read	FF	POR	ME	WD	OC	EE										

Register Read

The higher 6 bits contained in all the registers are fault flags, which always indicate critical faults. The remaining 10 bits read the individual settings of the corresponding register. The table below provides the definitions of the higher 6 bits.

Bit Name	Fault Description
FF	General fault flag
POR	V3 pin undervoltage (power-on reset)
ME	Memory error
WD	Watchdog timeout
OC	Soft overcurrent
EE	EEPROM overwrite limit

12. Design Notes

12.1. Notes on the Sequences for Turning On/Off the IC

The following must be taken into account in the sequences for turning on and off the IC.

- **Turning on**

In startup operations (incl. a restart), the following pins must be held at logic low until the V3 pin voltage is established: DIR, RESETn, SDA, and SCL. This low-level setting of the pins must also be applied to a restart from abnormalities in power supply, such as an instantaneous power failure. In particular, when applying external voltages on these pins, be sure to set the pins to logic low until the V3 pin voltage is established.

- **Turning off**

To turn off the IC, decrease the VSP pin voltage first, and then stop the motor operation.

12.2. PCB Pattern Layout

Figure 12-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

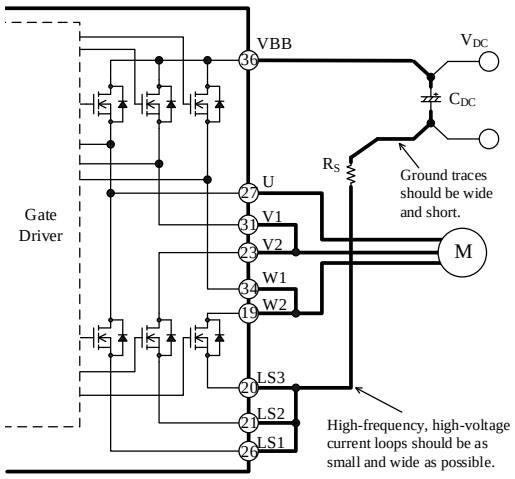


Figure 12-1. High-frequency, High-voltage Current Paths

12.3. Considerations in IC Characteristics Measurement

When measuring the leakage current of the output transistors (power MOSFETs) incorporated in the IC, note that all of the output (U, V1, W1), LSx, and COM pins must be appropriately connected. Otherwise, the output transistors may result in permanent damage. Also note that the gate and source of each output transistor should have the same potential during the leakage current measurement. Moreover, care should be taken during the measurement because each output transistor is connected as follows:

- All the high-side drains are internally connected to the VBB pin.
- In the U-phase, the high-side source and the low-side drain are internally connected to the U pin. (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)
- The high-side gates are internally pulled down to the output pins.
- The low-side gates are internally pulled down to the COM pin.

The following are circuit diagrams representing typical measurement circuits for leakage current: Figure 12-2 shows the high-side transistor (Q_{1H}) in the U-phase; Figure 12-3 shows the low-side transistor (Q_{1L}) in the U-phase. And all the pins that are not represented in these figures are open. When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LSx pin to be measured to the COM pin, then leave other unused pins open.

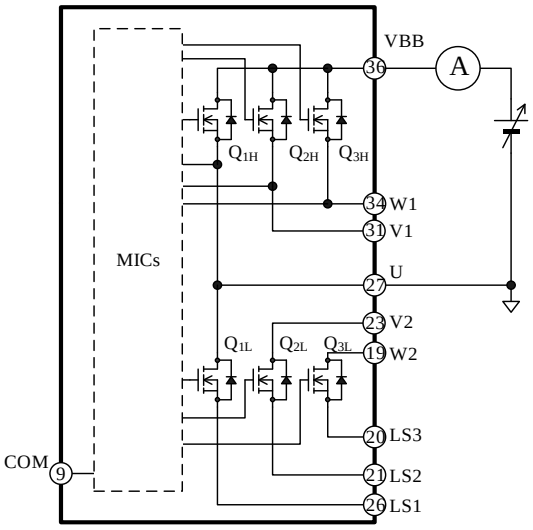


Figure 12-2. Typical Measurement Circuit for High-side Transistor (Q_{1H}) in U-phase

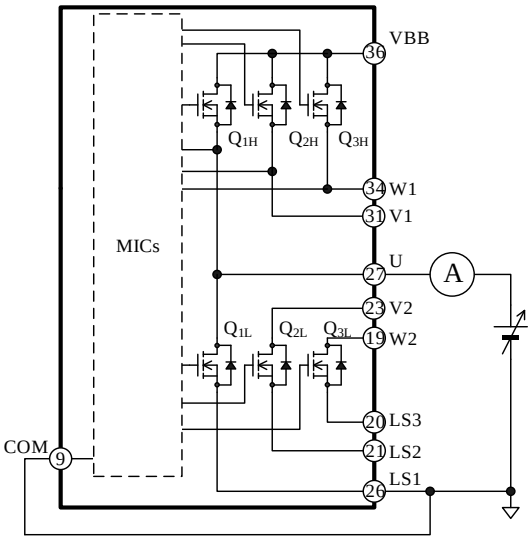


Figure 12-3. Typical Measurement Circuit for Low-side Transistor (Q_{1L}) in U-phase

13. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in output transistors (power MOSFETs), and to estimate a junction temperature. Note that the descriptions listed here are applicable to the IC, which is controlled by a 3-phase sine-wave PWM driving strategy. For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SX68200M Series Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, P_{RR}, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

13.1. Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-1, a linear approximation at a range the I_D is actually used is obtained by: $R_{DS(ON)} = \alpha \times I_D + \beta$.

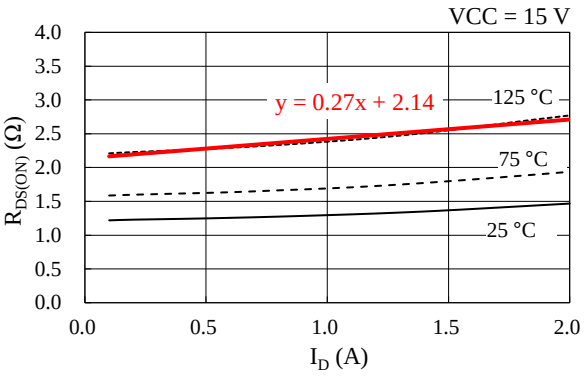


Figure 13-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D

The values gained by the above calculation are then applied as parameters in Equation (52), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) {I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) {I_M}^2 . \quad (52)$$

Where:

I_D is the drain current of the power MOSFET (A),

$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),

DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),

cosθ is the motor power factor (0 to 1),

I_M is the effective motor current (A),

α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and

β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

13.2. Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (53) or (54), letting I_M be the effective current value of the motor:

- **SX68201M**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{150}. \quad (53)$$

- **SX68203M / SX68204M / SX68205M**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (54)$$

Where:
f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBB pin input voltage, and
α_E is the slope on the switching loss curve (see Section 14.3.1.2).

13.3. Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-2, a linear approximation at a range the I_{SD} is actually used is obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

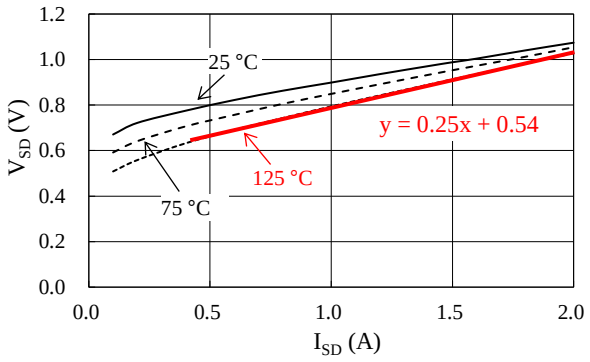


Figure 13-2. Linear Approximate Equation of V_{SD} vs. I_{SD}

The values gained by the above calculation are then applied as parameters in Equation (55), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (55)$$

Where:
V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
$\cos\theta$ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

13.4. Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (56):

$$T_J = R_{J-C} \times \{(P_{RON} + P_{SW} + P_{SD}) \times 6\} + T_C . \quad (56)$$

Where:
R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-3.

14. Performance Curves

14.1. Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

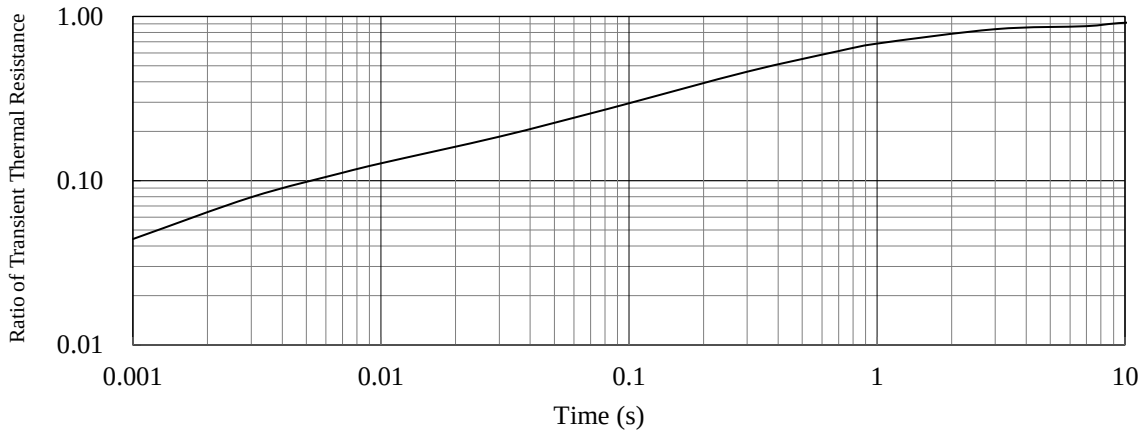


Figure 14-1. Transient Thermal Resistance: SX68201M

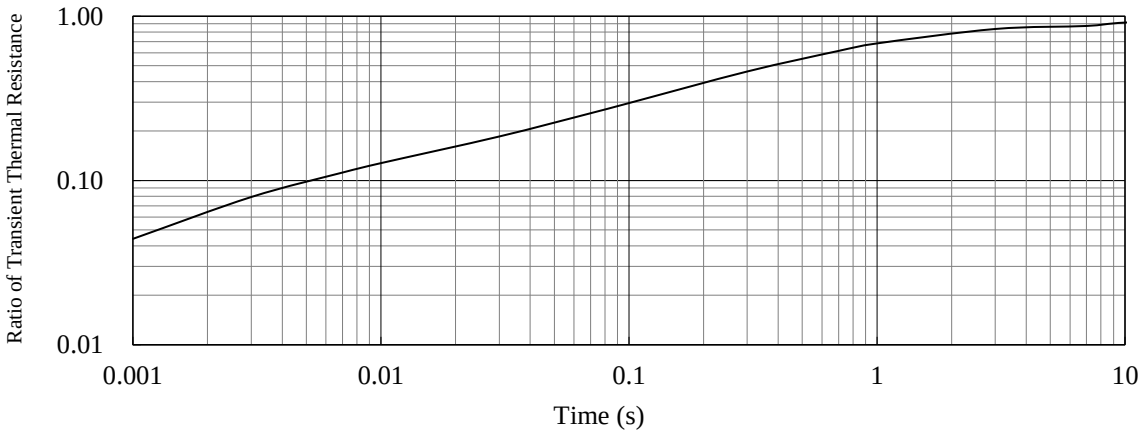


Figure 14-2. Transient Thermal Resistance: SX68203M

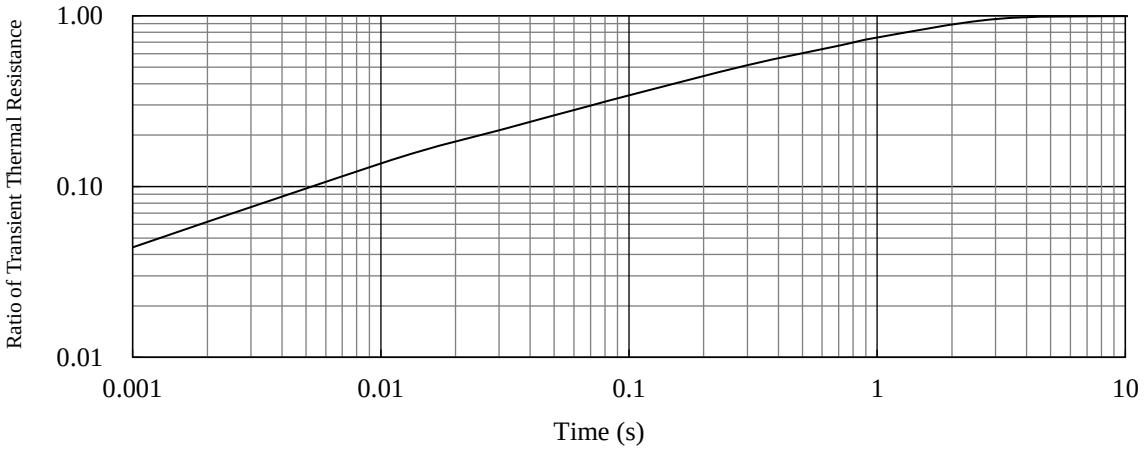


Figure 14-3. Transient Thermal Resistance: SX68204M

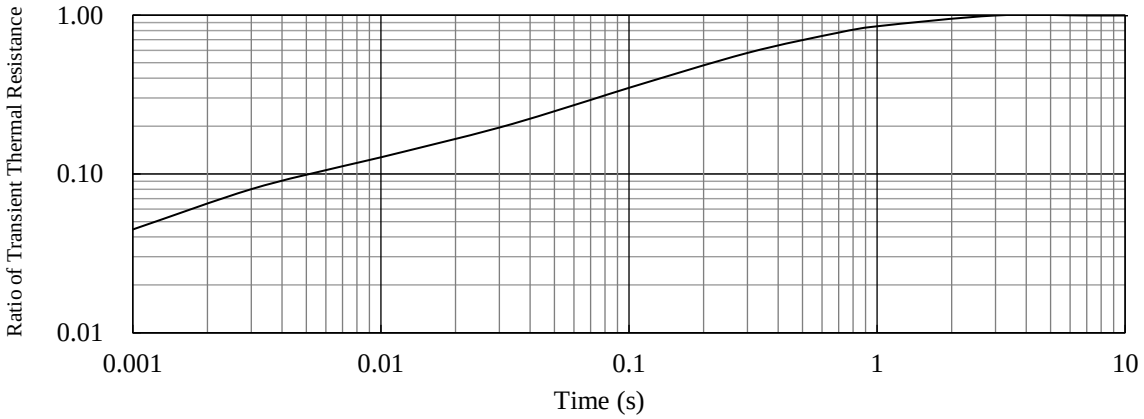


Figure 14-4. Transient Thermal Resistance: SX68205M

14.2. Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ and typical switching losses.

14.2.1. SX68201M

Operating conditions: VBB pin input voltage, V_{DC} = 150 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

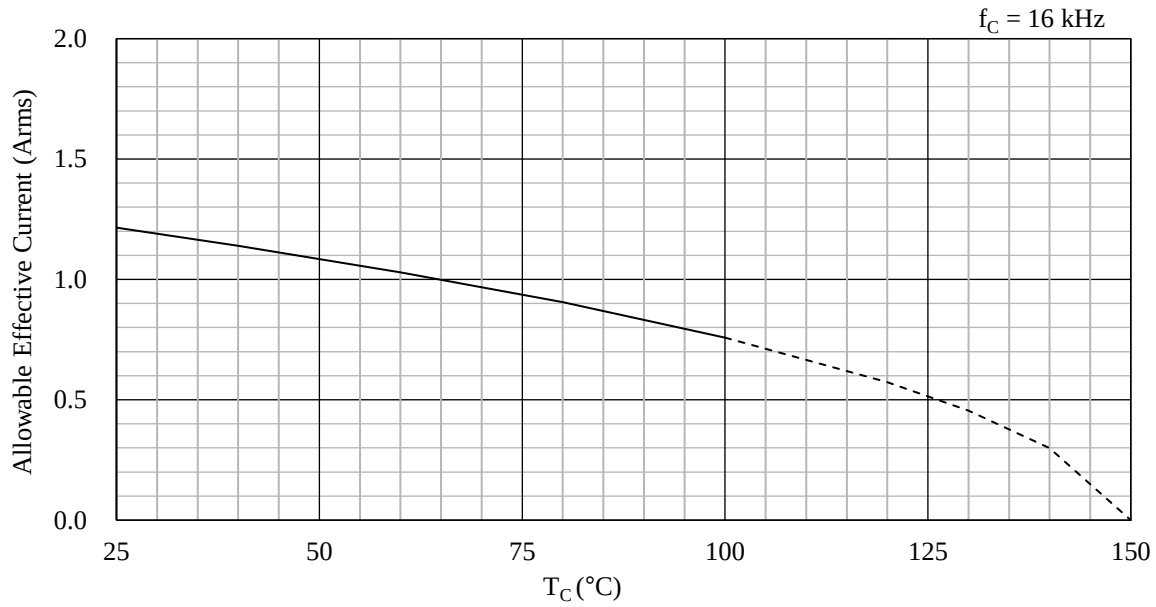


Figure 14-5. Allowable Effective Current (f_C = 16 kHz)

14.2.2. SX68203M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

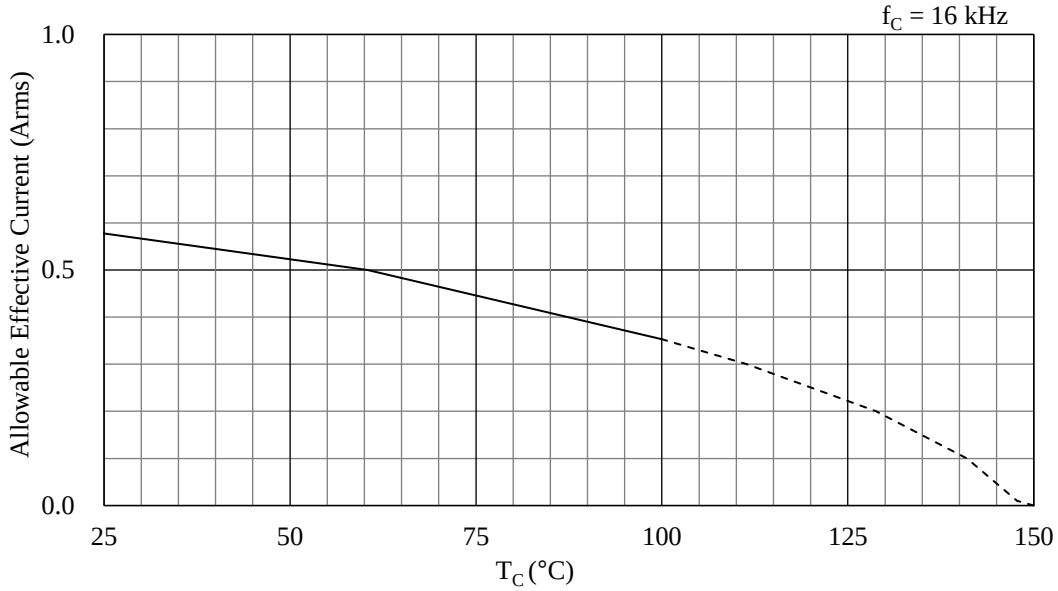


Figure 14-6. Allowable Effective Current (f_C = 16 kHz)

14.2.3. SX68204M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

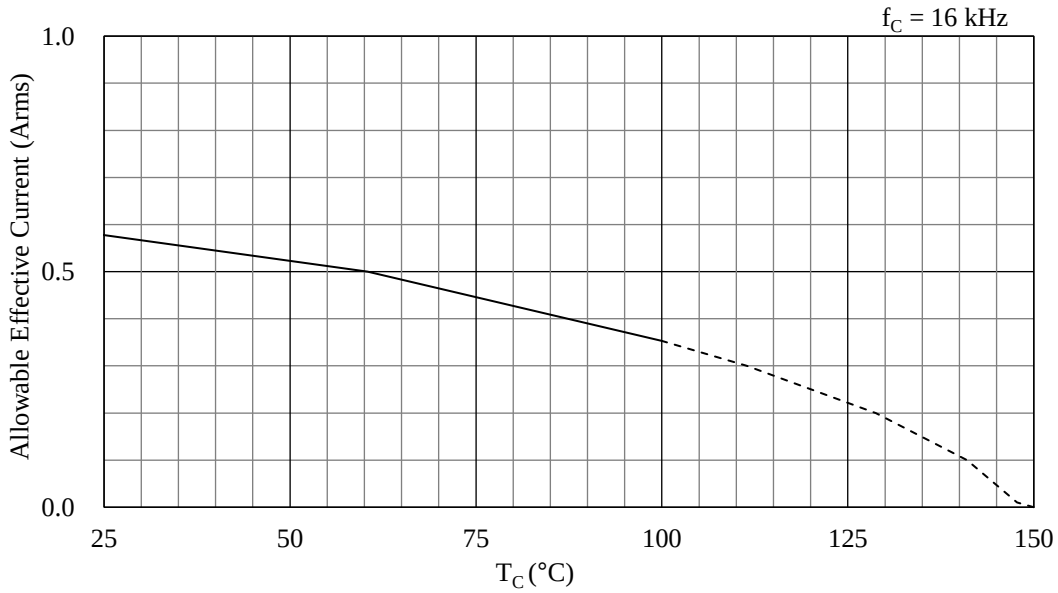


Figure 14-7. Allowable Effective Current (f_C = 16 kHz)

14.2.4. SX68205M

Operating conditions: VBB pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

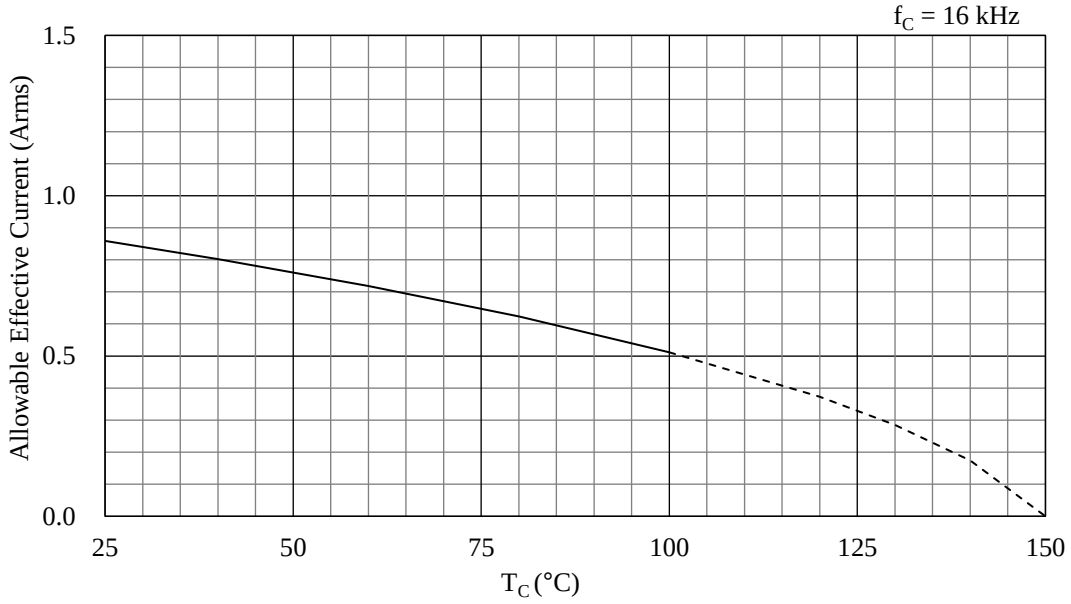


Figure 14-8. Allowable Effective Current (f_C = 16 kHz)

14.3. Performance Curves of Output Parts

14.3.1. Output Transistor Performance Curves

14.3.1.1. SX68201M

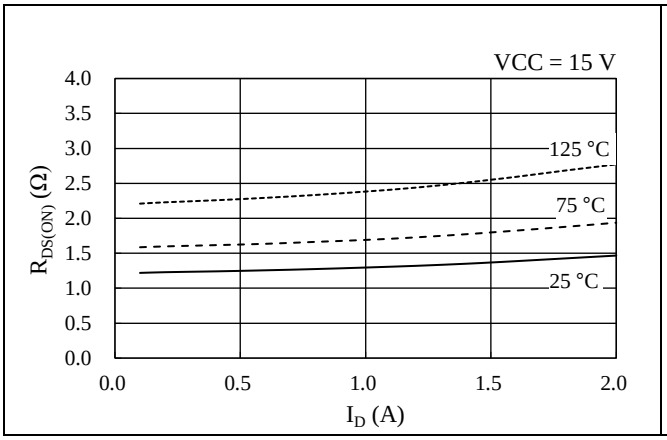


Figure 14-9. Power MOSFET $R_{DS(ON)}$ vs. I_D

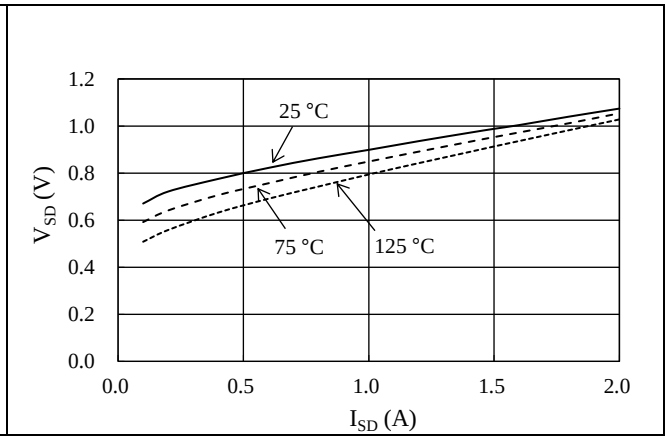


Figure 14-10. Power MOSFET V_{SD} vs. I_{SD}

14.3.1.2. SX68203M

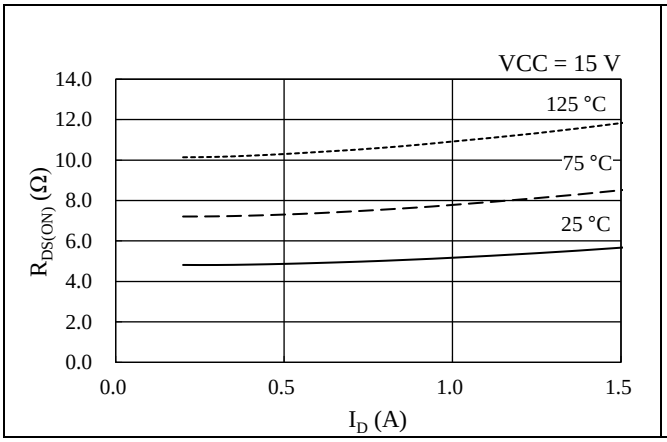


Figure 14-11. Power MOSFET $R_{DS(ON)}$ vs. I_D

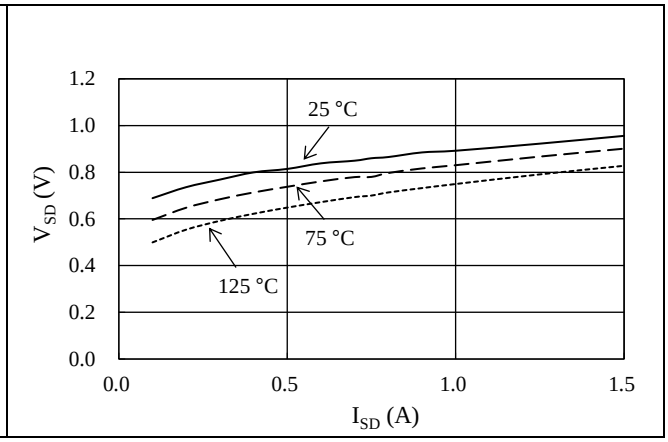


Figure 14-12. Power MOSFET V_{SD} vs. I_{SD}

14.3.1.3. SX68204M

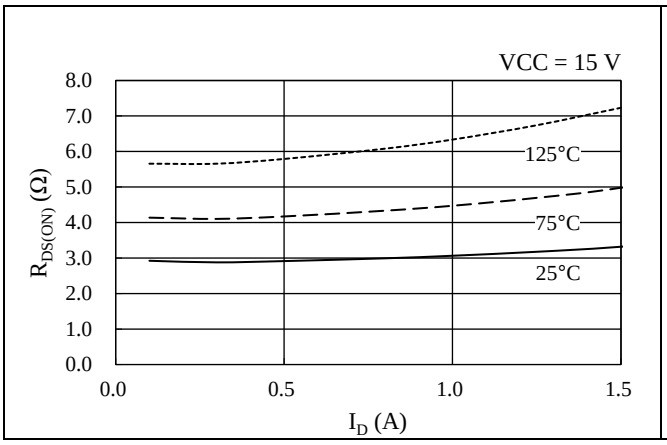


Figure 14-13. Power MOSFET $R_{DS(ON)}$ vs. I_D

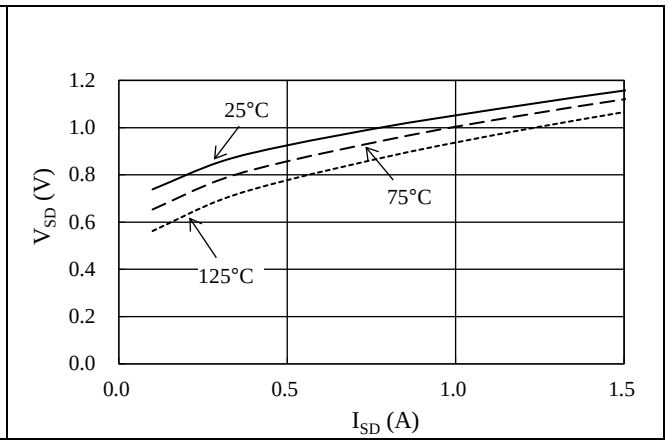


Figure 14-14. Power MOSFET V_{SD} vs. I_{SD}

14.3.1.4. SX68205M

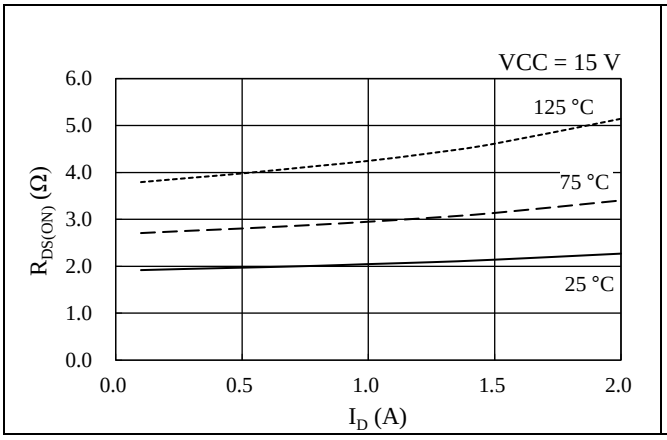


Figure 14-15. Power MOSFET $R_{DS(ON)}$ vs. I_D

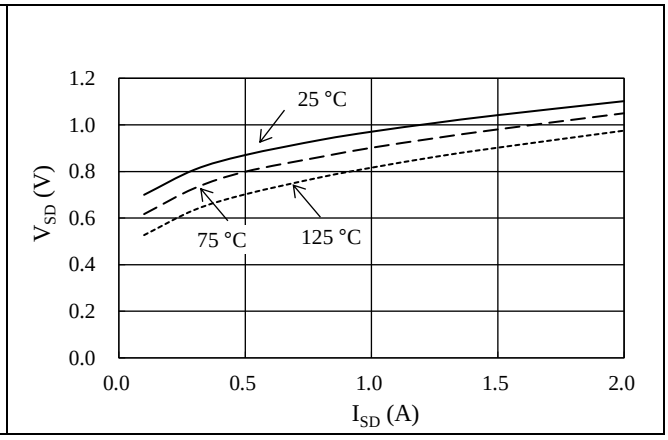


Figure 14-16. Power MOSFET V_{SD} vs. I_{SD}

14.3.2. Switching Loss Curves

14.3.3. SX68201M

Conditions: VBB pin voltage = 150 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

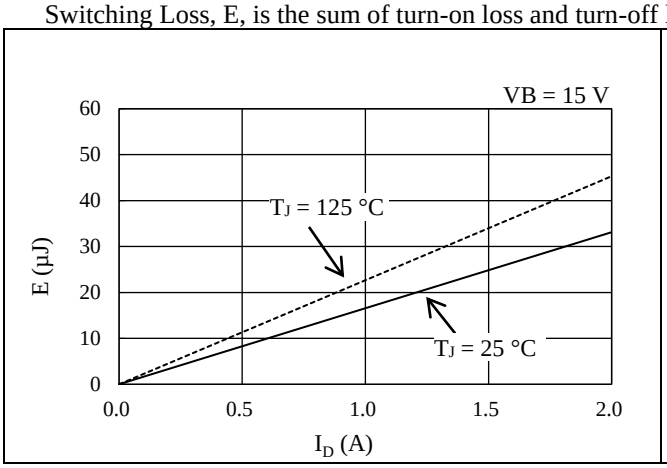


Figure 14-17. High-side Switching Loss

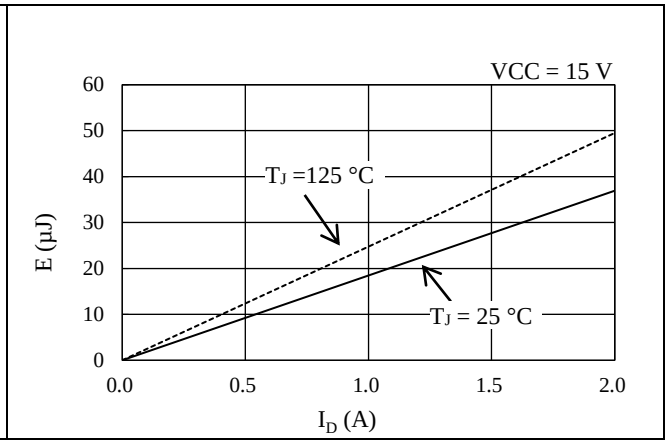


Figure 14-18. Low-side Switching Loss

14.3.4. SX68203M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

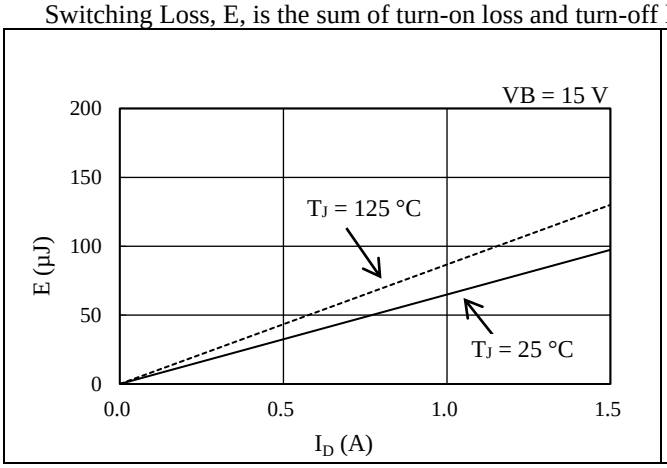


Figure 14-19. High-side Switching Loss

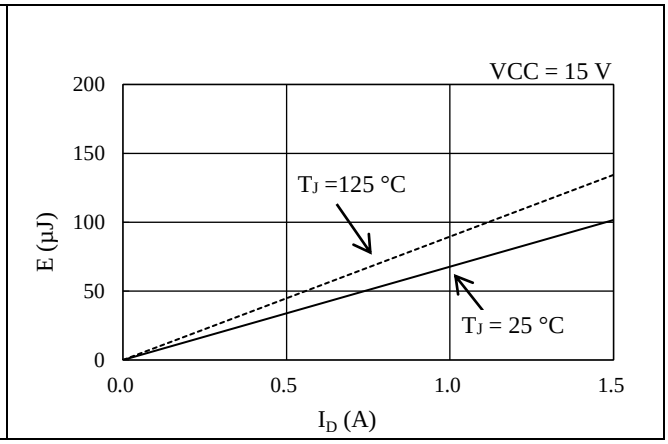


Figure 14-20. Low-side Switching Loss

14.3.5. SX68204M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

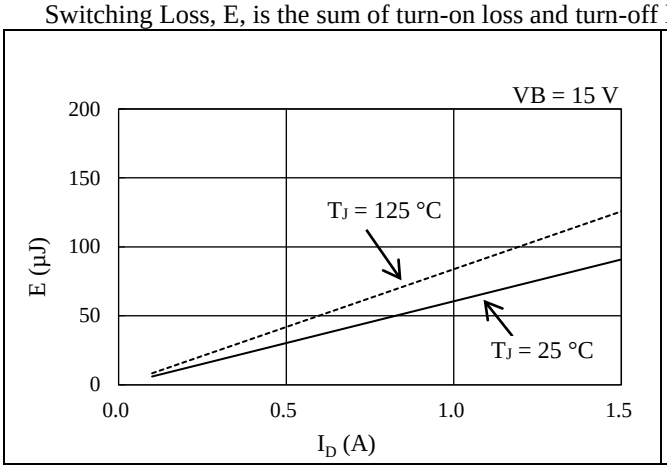


Figure 14-21. High-side Switching Loss

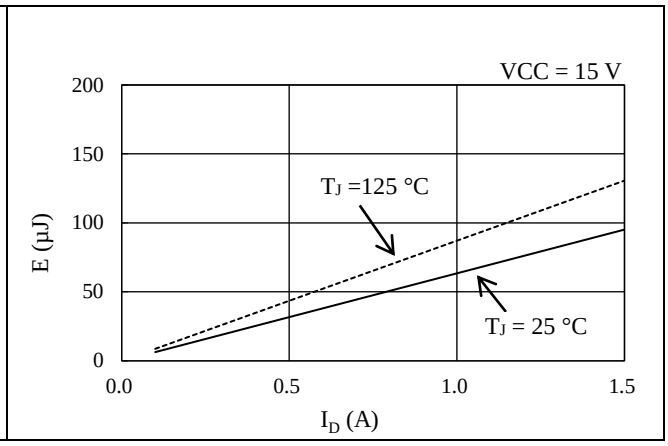


Figure 14-22. Low-side Switching Loss

14.3.6. SX68205M

Conditions: VBB pin voltage = 300 V, half-bridge circuit with inductive load.
Switching Loss, E, is the sum of turn-on loss and turn-off loss.

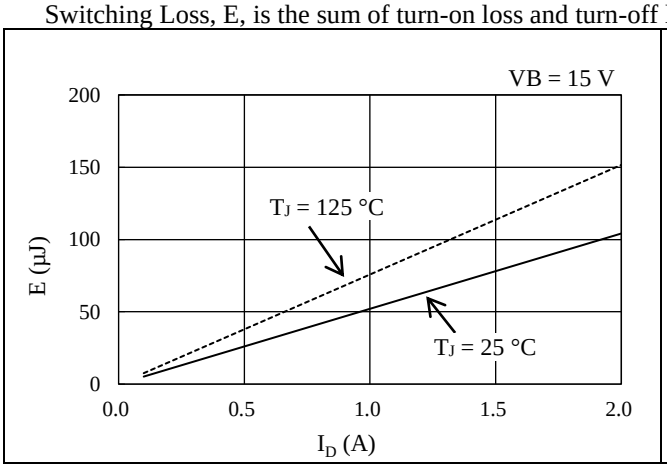


Figure 14-23. High-side Switching Loss

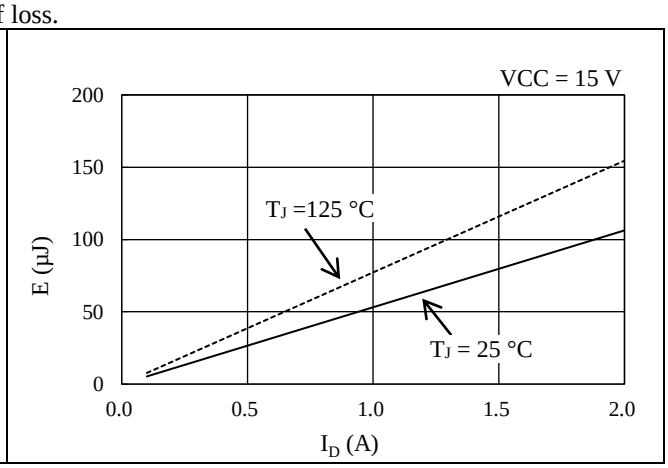
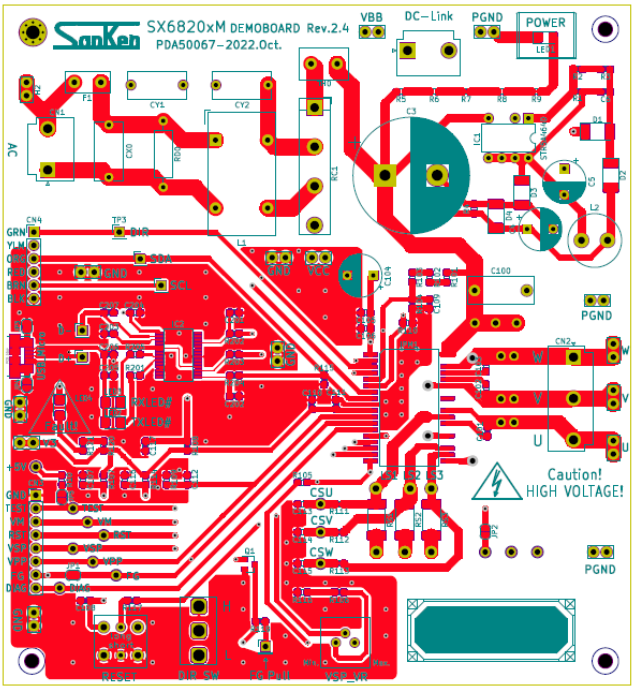


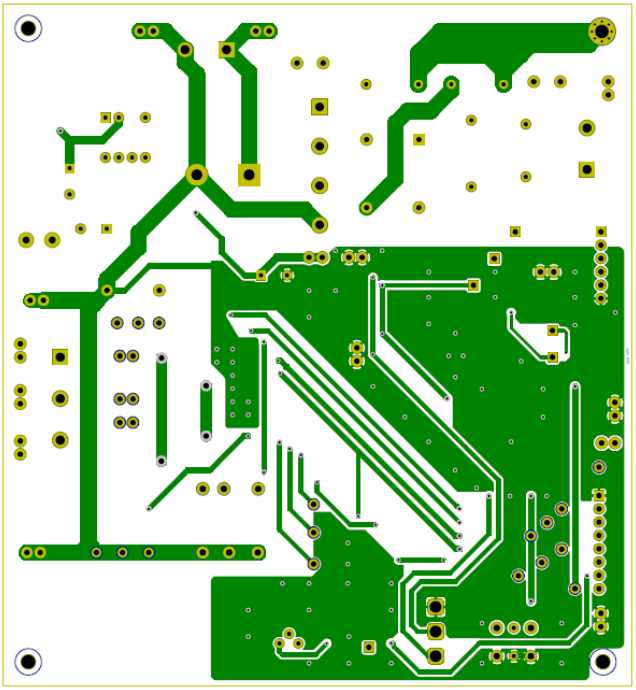
Figure 14-24. Low-side Switching Loss

15. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SX68200M series device. Note that the pattern layout example only uses the parts illustrated in the circuit diagram below. For details on the land pattern example of the IC, see Section 9.



(Top View)



(Bottom View)

Figure 15-1. Pattern Layout Example

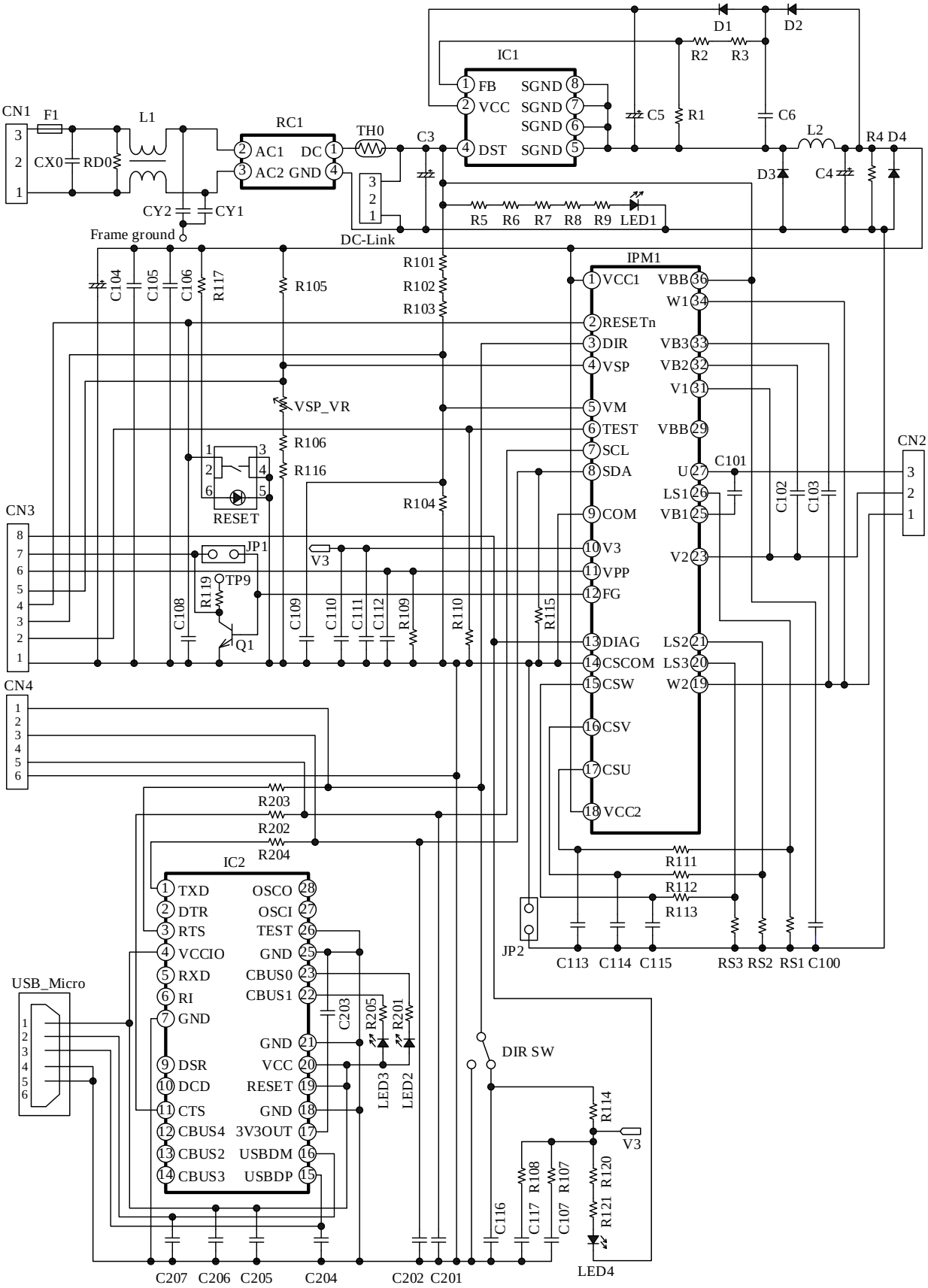


Figure 15-2. Circuit Diagram of PCB Pattern Layout Example

16. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SX68203M
Main Supply Voltage, V_{DC}	280 VDC (typ.)
Rated Output Power	30 W

- **Circuit Diagram**

See Figure 15-2.

● **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C3	Electrolytic	120 µF, 400 V	R109*	General	Open
C4	Electrolytic	100 µF, 25 V	R110	General	10 kΩ, 0.25 W
C5	Electrolytic	10 µF, 50 V	R111	General	100 Ω, 0.25 W
C6	Ceramic	0.22 µF, 50 V	R112	General	100 Ω, 0.25 W
C100	Film	0.047 µF, 400 V	R113	General	100 Ω, 0.25 W
C101	Ceramic	1 µF, 50 V	R114	General	10 kΩ, 0.25 W
C102	Ceramic	1 µF, 50 V	R115	General	10 kΩ, 0.25 W
C103	Ceramic	1 µF, 50 V	R116	General	2.2 kΩ, 0.25 W
C104	Electrolytic	100 µF, 25 V	R117	General	Open
C105	Ceramic	1 µF, 50 V	R119	General	3.3 kΩ, 0.25 W
C106	Ceramic	1 µF, 50 V	R120	General	10 kΩ, 0.25 W
C107	Ceramic	100 pF, 50 V	R121	General	10 kΩ, 0.25 W
C108*	Ceramic	Open	R201	General	1 kΩ, 0.25 W
C109	Ceramic	0.1 µF, 50 V	R202	General	100 Ω, 0.25 W
C110	Ceramic	1 µF, 50 V	R203	General	Open
C111	Ceramic	0.1 µF, 50 V	R204	General	100 Ω, 0.25 W
C112	Ceramic	0.1 µF, 50 V	R205	General	1 kΩ, 0.25 W
C113	Ceramic	1000 pF, 50 V	RS1*	Metal plate	0.36 Ω, 1 W
C114	Ceramic	1000 pF, 50 V	RS2*	Metal plate	0.36 Ω, 1 W
C115	Ceramic	1000 pF, 50 V	RS3*	Metal plate	0.36 Ω, 1 W
C116	Ceramic	100 pF, 50 V	RD0	Metal plate	1 MΩ, 1 W
C117	Ceramic	100 pF, 50 V	TH0	Thermistor	10 Ω, 1800 mW
C201*	Ceramic	Open	VSP_VR	Trimmer	20 kΩ, 0.5 W
C202*	Ceramic	Open	D1	Fast recovery	200 V, 1 A
C203	Ceramic	0.1 µF, 50 V	D2	Fast recovery	500 V, 1 A
C204	Ceramic	Open	D3	Fast recovery	500 V, 1 A
C205	Ceramic	1 µF, 50 V	D4	Zener diode	1 W, Vz = 18.8 V (min.)
C206	Ceramic	0.1 µF, 50 V	L1	Filter	74.5 mH
C207	Ceramic	Open	L2	Inductor	1 mH
CX0	Film	22 nF, 275 VAC	F1	Fuse	250 VAC, 1 A
CY1	Ceramic	4.7 nF, 250 VAC	LED1	LED	5 V, 30 mA
CY2	Ceramic	4.7 nF, 250 VAC	LED2	LED	5 V, 30 mA
R1	General	10 kΩ, 0.25 W	LED3	LED	5 V, 30 mA
R2	General	47 kΩ, 0.25 W	LED4	LED	5 V, 30 mA
R3	General	4.7 kΩ, 0.25 W	RESET	Switch	TS-AGGNH-G
R4	General	4.7 kΩ, 0.25 W	DIR SW	Switch	1MS1-T2-B1-M1-Q-N-S
R5	General	33 kΩ, 0.25 W	USB_Micro	Micro USB Type-b connector	ZX62-B-5PA
R6	General	33 kΩ, 0.25 W	CN1	Connector	Equiv. to B2P3-VH
R7	General	33 kΩ, 0.25 W	CN2	Connector	Equiv. to B3P5-VH
R8	General	33 kΩ, 0.25 W	CN3	Pin header	2.54 mm pitch
R9	General	33 kΩ, 0.25 W	CN4	Pin header	2.54 mm pitch
R101	Metal plate	1 MΩ, 0.25 W	DC-Link	Connector	Equiv. to B2P3-VH
R102	Metal plate	1 MΩ, 0.25 W	RC1	Bridge diode	D3SBA60
R103	Metal plate	1 MΩ, 0.25 W	Q1	NPN transistor	Open
R104	Metal plate	10 kΩ, 0.25 W	IPM1	IC	SX68203M
R105	General	47 kΩ, 0.25 W	IC1	IC	STR5A464D
R106	General	5.6 kΩ, 0.25 W	IC2	IC	FT232RL
R107	General	10 kΩ, 0.25 W	JP1	Jumper	Short
R108	General	10 kΩ, 0.25 W	JP2	Jumper	Short

* Refers to a part that requires adjustment based on operation performance in an actual application.

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