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# Graphic Display Module

## Part Number

G123AXGFGSW6WN55AAC

## Overview

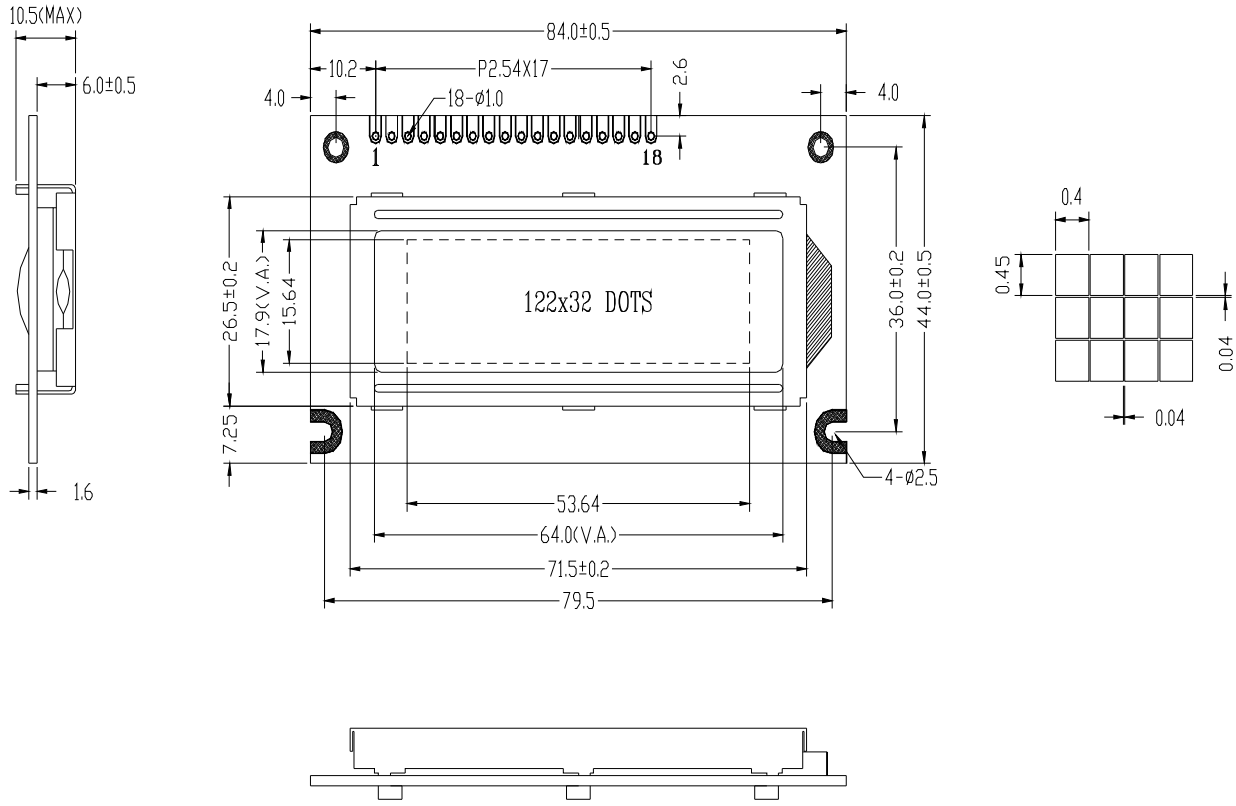
122x32(84x44), FSTN, White Edge lit, Bottom view, Wide temp, Transmissive (negative), 5V LCD, 3.1V LED, Controller=SBN1661G, RoHS Compliant

**G123AXGFGSW6WN55AAC**

## Features

1、Full dot-matrix structure with 122 x 32 dots
2、Built-in controller (SBN1661G_M18-D or Equivalent)
3、Power supply VDD=5V
4、1/32 duty ,1/6 bias
5、FSTN, negative, transmissive,
6、LED Side light (White)
7、6 o'clock viewing angle
8、8 bits parallel data input

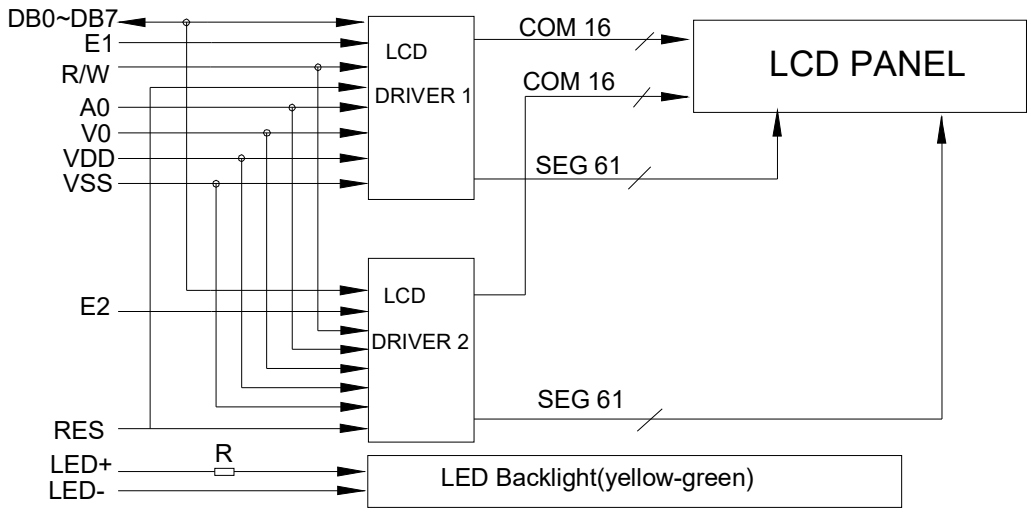
## Mechanical diagram (Unit: mm )




## Absolute Maximum Ratings

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Voltage | $V_{DD}$ -$V_{SS}$ | 0 | 7.0 | V |
| Input Voltage | $V_O$ | $V_{SS}$ | $V_{DD}$ | |
| Operating Temperature Range | $T_{OP}$ | -20 | +70 | ℃ |
| Storage Temperature Range | $T_{ST}$ | -30 | +80 | |

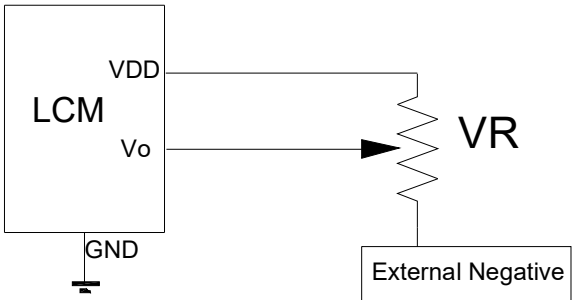
## Block diagram




## Description Of Terminals

| Pin No. | Pin Name | Input/ Output | External Connection | Function |
|---|---|---|---|---|
| 1 | VSS | — | Power Supply | Signal ground for LCM |
| 2 | VDD | — | | VDD: +5V |
| 3 | VO | — | | $V_{LCD}$ adjustment |
| 4 | RST | Output | MPU | Reset signal |
| 5 | E1 | Input | MPU | Enable clock input, SEG(1~61) |
| 6 | E2 | Input | MPU | Enable clock input, SEG(62~122) |
| 7 | R/W | Input | MPU | Read/write select signal<br>“0” for writing, “1” for reading |
| 8 | A0 | Input | MPU | Register select input<br>“0”:Instruction register (when writing)<br>Busy flag address counter (When reading)<br>“1”:Data register (when writing & reading) |
| 9~16 | DB0-DB7 | Input/output | MPU | Data bus [0~7] Bi-directional data bus |
| 17 | LED+ | — | LED BK Power supply | Power supply for BKL (+5.0V) |
| 18 | LED- | — | | Power supply for BKL (GND) |

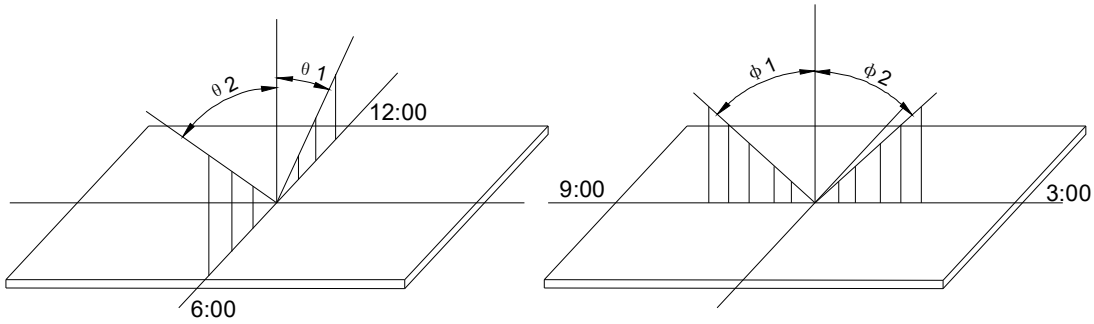
## Contrast adjust




VDD-Vo:LCD DRIVING VOLTAGE

VR:10K~20K

## Optical characteristics

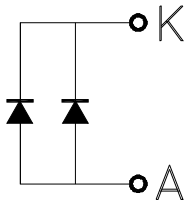



FSTN type display module (Ta=25℃, VDD=5.0V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Viewing angle | θ 1 | Cr≥3 | | 20 | | deg |
| | θ 2 | | | 40 | | |
| | Φ1 | | | 35 | | |
| | Φ2 | | | 35 | | |
| Contrast ratio | Cr | | - | 6 | - | - |
| Response time (rise) | Tr | - | - | 200 | 250 | ms |
| Response time (fall) | Tr | - | - | 300 | 350 | |

## Electrical characteristics

### LED backlight circuit (color: white)




### LED ratings

| ITEM | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| FORWARD VOLTAGE | VF | 2.9 | 3.1 | 3.4 | V |
| FORWARD CURRENT | IF | - | 20 | 40 | MA |
| POWER | P | - | - | 0. 2 | W |
| PEAK WAVE LENGTH | ΛP | - | - | - | NM |
| LUMINANCE | LV | - | 200 | - | CD/M2 |

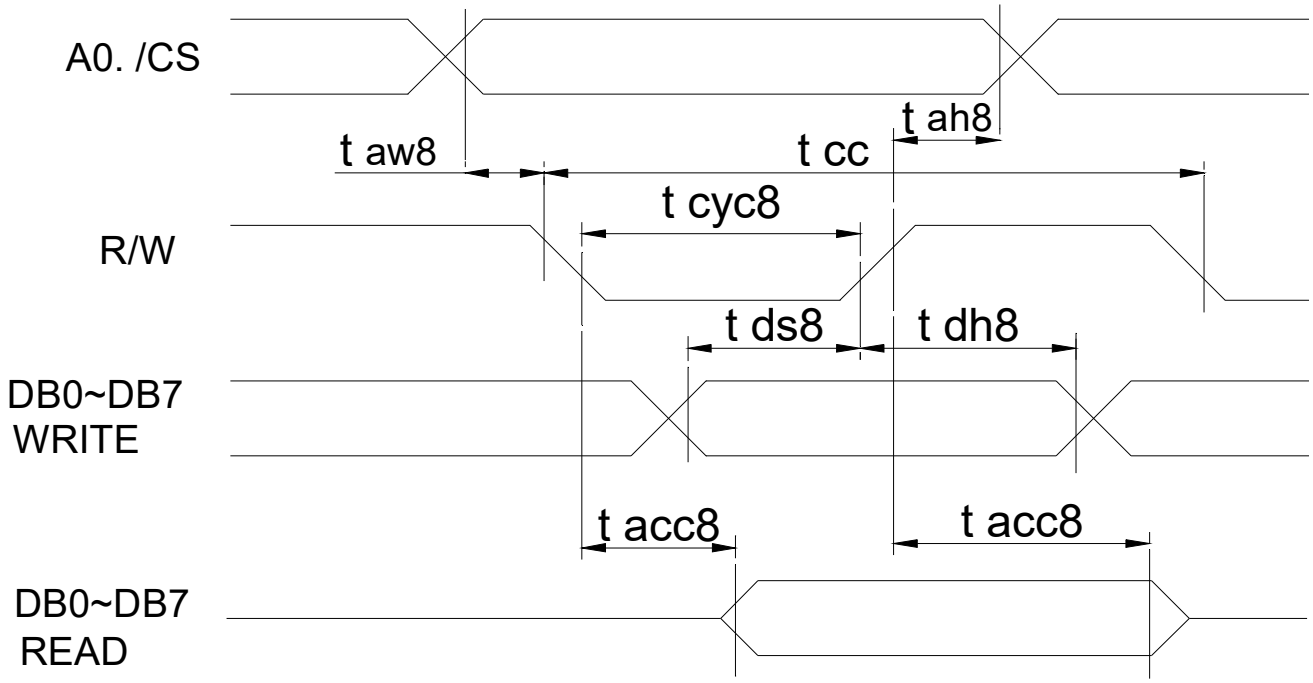
DC characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage for LCD | $V_{DD}$-$V_0$ | Ta =25℃ | - | 6.5 | - | V |
| Input voltage | $V_{DD}$ | | 4.8 | 5.0 | 5.3 | |
| Backlight supply voltage | $V_F$ | | - | | 5.0 | |
| Supply current | $I_{DD}$ | Ta=25℃, $V_{DD}$=5.0V | - | 1.5 | 2.5 | mA |
| Backlight supply current | $I_F$ | V=5.0V,R=100 ohm | - | 20 | 40 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LKG}$ | | - | - | 1.0 | uA |
| “H” level input voltage | $V_{IH}$ | | 2.2 | - | $V_{DD}$ | V |
| “L” level input voltage | $V_{IL}$ | Twice initial value or less | 0 | - | 0.6 | |
| “H” level output voltage | $V_{OH}$ | LOH=-0.25mA | 2.4 | - | - | |
| “L” level output voltage | $V_{OL}$ | LOH=1.6mA | - | - | 0.4 | |

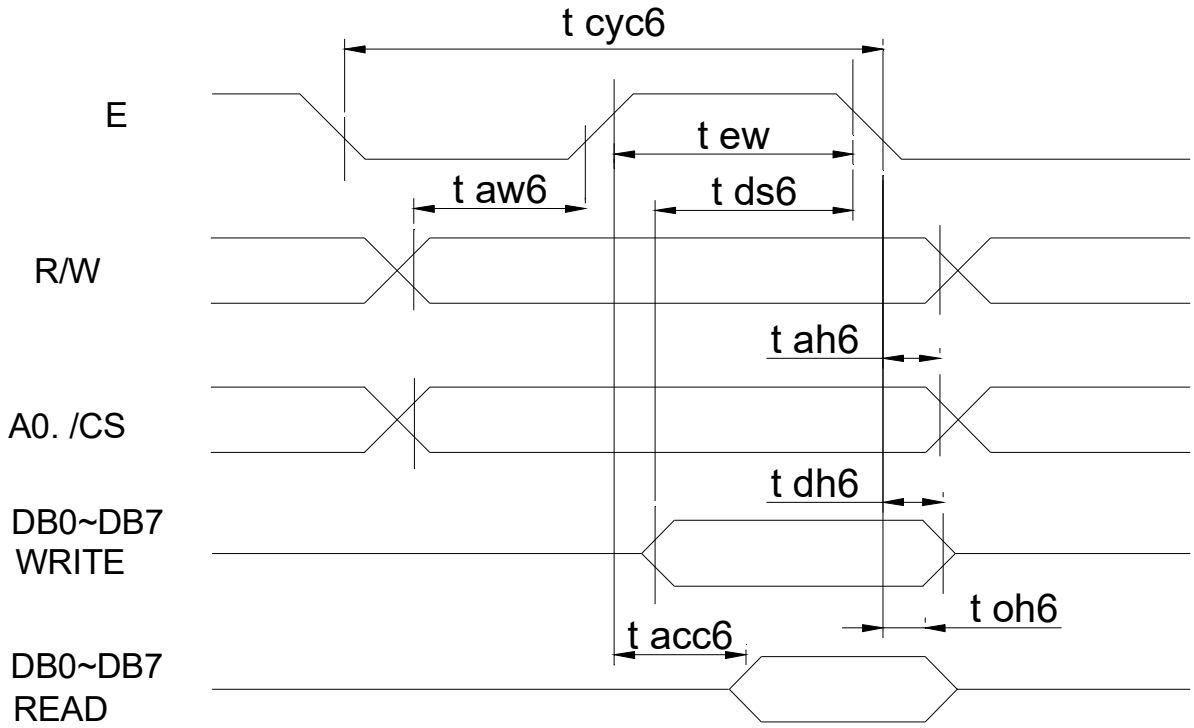
## Timing Characteristics

### MPU bus read/write 1(80-family MPU)




| Item | symbol | Conditions | Min. | Max. | unit |
|---|---|---|---|---|---|
| System cycle time | t cyc | — | 1000 | — | ns |
| Address setup time | t aw8 | — | 20 | — | ns |
| Address hold time | t ah8 | — | 10 | — | ns |
| Data setup time | t ds8 | — | 80 | — | ns |
| Data hold time | t dh8 | — | 10 | — | ns |
| Control pulse width | t cc8 | — | 200 | — | ns |
| RD access time | t cc8 | CL=100pf | — | 90 | ns |
| Output disable time | t ch8 | | 10 | 60 | ns |

## MPU bus read/write 2(68-family MPU)




| Item | | symbol | Conditions | Min. | Max. | unit |
|---|---|---|---|---|---|---|
| System cycle time | | t cyc6 | — | 1000 | — | ns |
| Address setup time | | t aw6 | — | 20 | — | ns |
| Address hold time | | t ah6 | — | 10 | — | ns |
| Data setup time | | t ds6 | — | 80 | — | ns |
| Data hold time | | t dh6 | — | 10 | — | ns |
| Access time | | t acc6 | CL=100pf | — | 90 | ns |
| Output disable time | | t oh6 | | 10 | 60 | ns |
| Enable pulse width | Read | t ew | — | 100 | — | ns |
| | Write | | — | 80 | — | ns |

## Display command

| Parameter | A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display ON /OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | Turns display on or off 1: ON ; 0 : OFF |
| Display start line | 0 | 1 | 0 | 1 | 1 | 0 | Display start address (0 to 31) | | | | | Specifies RAM line corresponding to top line of display |
| Set page address | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Page (0 to 3) | | Sets display RAM page in page address register |
| Set column (segment) address | 0 | 1 | 0 | 0 | Column address (0 to 79) | | | | | | | Sets display RAM column address in column address register |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read status | 0 | 0 | 1 | Bu sy | A D C | ON/ OFF | R E S E T | 0 | 0 | 0 | 0 | Reads the following status:<br>BUSY 1: Busy 0: Ready<br>ADC 1: CW output 0: CCW output<br>ON/OFF 1: Display off 0: Display on<br>RESET 1: Being reset 0: Normal |
| Write display data | 1 | 1 | 0 | Write data | | | | | | | | Write data from data bus into display RAM |
| Read Display data | 1 | 0 | 1 | Read data | | | | | | | | Read data from display RAM onto data bus |
| Select ADC | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | 0: CW output 1: CCW output |
| Static driver ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | Selects static driving operation.<br>1: static driver, 0: Normal driving |
| Select duty | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0/1 | Select LCD duty cycle<br>1: 1/32, 0: 1/16 |
| Read-modify write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Read-modify-write ON |
| End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Read-modify-write OFF |
| Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Software reset |

Note: The SBN1661G series identifies a data bus using a combination of A0 and R/W (RD or WR signals. As the MPU translates a command in the internal timing only (independent from the external clock). Its speed is very high. The busy check is usually not required.

**Display ON/OFF (AEH, AFH)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D |

The command turns the display on and off
D=1: display ON D=0: display OFF

**Display start line (C0H~DFH)**

This command specifies the line address and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command the vertical smooth scrolling and paging can be used.

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | A4 | A3 | A2 | A1 | A0 |

This command loads the display start line register.

| A4 | A3 | A2 | A1 | A0 | Line address |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| / | / | / | / | / | / |
| 1 | 1 | 1 | 1 | 1 | 1F |

**Set page address (B8H~BBH)**

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | A1 | A0 |

This command loads the page address register.

| A1 | A0 | Page |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

**Set column address (00H~4FH)**

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

This command loads the column address register.

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | Column address |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| / | / | / | / | / | / | / | / |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F |

**Read status**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | Busy | ADC | On/off | Reset | A3 | A2 | A1 | A0 |

Reading the command I/O register (A0=0) yields system status information.
The busy bit indicates whether the driver will accept a command or not.
Busy=1: the driver is currently executing a command or is resetting. No new command will be accepted.
Busy=0: the driver will accept a new command.
The ADC bit indicates the way column addresses are assigned to segment drivers.
ADC=1 Normal. Column address n→ segment driver n.
ADC=0 Inverted. Column address 79 u→ segment driver u.
The ON/OFF bit indicates the current status of the display.
It is the inverse of the polarity of the display ON/OFF command.
ON/OFF=1: display off
ON/OFF=0: display on
The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
Reset=1: currently executing reset command.
Reset=0: normal operation

**Write display data**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | Write data | | | | | | | |

Writes 8-bit of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

**Read display data**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | Read data | | | | | | | |

Reads 8-bit of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

**Select ADC (A0H, A1H)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D |

This command selects the relationship between display data RAM column addresses and segment drivers.

D=1: SEG0← column address 4FH,4EH…00H(inverted).

D=0: SEG0← column address 00H,01H…4FH(normal).

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design.

**Static drive ON/OFF (A4H, A5H)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

Forces display on and all common outputs to be selected.

D=1:static drive on

D=0:static drive off

**Select duty (A8H; A9H)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D |

This command sets the duty cycle of the LCD drive and is only valid for the SBN1661G.it is invalid for the SBN0080G, which performs passive operation. The duty cycle of the SBN0080G is determined by the externally generated FR signal.

SBN1661G

D=1: 1/32 duty cycle

D=0: 1/16 duty cycle

When using the SBN1661G (having a built-in oscillator) and the SBN0080G continuously, set the duty as follows:

| | | SBN0080G |
|---|---|---|
| SBN1661G | 1/32 | 1/32 |
| | 1/16 | 1/16 |

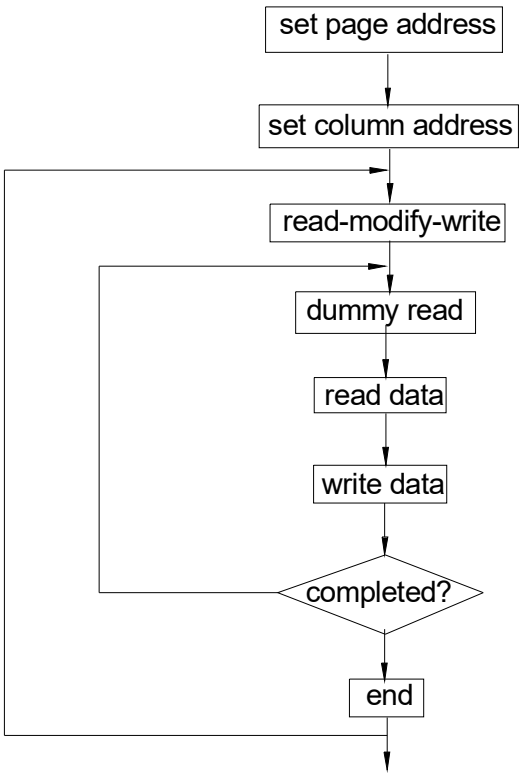
**READ-MODIFY-WRITE (E0H)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an end command is repeated. Operation sequence during cursor display

When the end command is entered, the column address is returned to the one used during input of read-modify-write command. This function can reduce the load of MPU when data change is repeated at a specific Display area (such as cursor blinking).

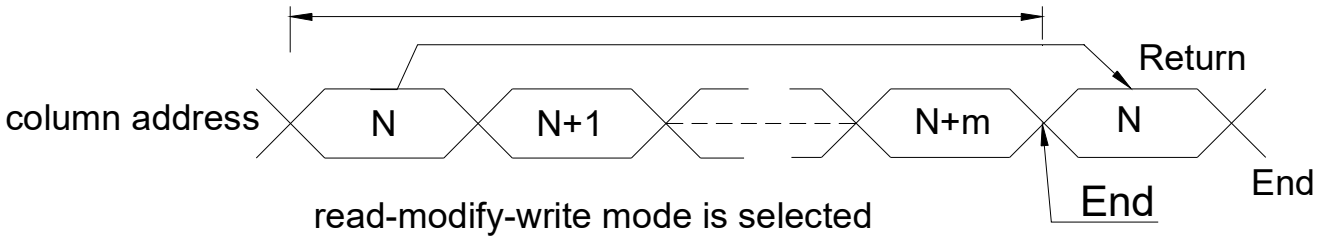
*Any command other than data read or write can be used in the read-modify-write mode. However, the column address set command cannot be used.




**END (EEH)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

ss




**RESET (E2H)**

| A0 | E (RD) | R/W (/WR) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

This command clears
The display start line register.
And set page address register to 3 page.
It does not affect the contents of the display data RAM.