

## PerFET™ Power Transistor

### FEATURES

- Excellent FOM
- AEC-Q101 Qualified
- Wettable Flank leads for Enhanced AOI
- 100% UIS and Rg tested
- 175°C Operating Junction Temperature
- RoHS Compliant
- Halogen-Free

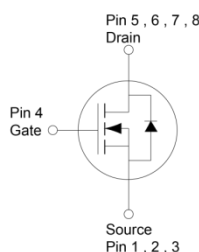
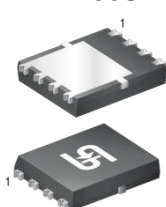
### APPLICATIONS

- Automotive Applications
- Solenoid and Motor Drivers
- DC-DC Converter

PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
$V_{DS}$	40	V	
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	5.6	mΩ
	$V_{GS} = 4.5V$	7.8	
$Q_g$	$V_{GS} = 4.5V$	14.2	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Continuous Drain Current, Silicon limited	$T_C = 25^\circ\text{C}$ $I_D$	90	A
Continuous Drain Current <sup>(Note 1)</sup>	$T_C = 25^\circ\text{C}$ $I_D$	54	A
	$T_C = 100^\circ\text{C}$ $I_D$	54	
	$T_A = 25^\circ\text{C}$ $I_D$	17	
Pulsed Drain Current	$I_{DM}$	216	A
Single Pulse Avalanche Current <sup>(Note 2)</sup>	$I_{AS}$	21	A
Single Pulse Avalanche Energy <sup>(Note 2)</sup>	$E_{AS}$	66.2	mJ
Total Power Dissipation	$T_C = 25^\circ\text{C}$ $P_D$	78.9	W
	$T_C = 125^\circ\text{C}$ $P_D$	26.3	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	1.9	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$

Note:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	$BV_{DSS}$	40	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.4	1.8	2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 16\text{V}, V_{DS} = 0\text{V}$	$I_{GSS}$	--	--	$\pm 100$	nA
Drain-Source Leakage Current	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$	$I_{DSS}$	--	--	1	$\mu\text{A}$
	$V_{GS} = 0\text{V}, V_{DS} = 40\text{V}$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10\text{V}, I_D = 27\text{A}$	$R_{DS(on)}$	--	4	5.6	m $\Omega$
	$V_{GS} = 4.5\text{V}, I_D = 27\text{A}$		--	5.3	7.8	
Forward Transconductance (Note 3)	$V_{DS} = 10\text{V}, I_D = 7\text{A}$	$g_{fs}$	--	117.5	--	S
<b>Dynamic</b>						
Total Gate Charge	$V_{GS} = 4.5\text{V}, V_{DS} = 20\text{V},$ $I_D = 17\text{A}$	$Q_g$	--	14.2	21.3	nC
Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 17\text{A}$	$Q_g$	--	30.4	45.6	
Gate-Source Charge		$Q_{gs}$	--	5.7	11.4	
Gate-Drain Charge		$Q_{gd}$	--	4.6	9.2	
Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V},$ $f = 1.0\text{MHz}$	$C_{iss}$	--	1945	2918	pF
Output Capacitance		$C_{oss}$	--	331	662	
Reverse Transfer Capacitance		$C_{rss}$	--	45	90	
Gate Resistance	$f = 1.0\text{MHz}$	$R_g$	--	1.6	--	$\Omega$
<b>Switching</b> (Note 4)						
Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 20\text{V},$ $I_D = 17\text{A}, R_G = 1.5\Omega$	$t_{d(on)}$	--	8.2	--	ns
Rise Time		$t_r$	--	54.3	--	
Turn-Off Delay Time		$t_{d(off)}$	--	24.6	--	
Fall Time		$t_f$	--	5.7	--	
<b>Source-Drain Diode</b>						
Diode Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 27\text{A}$	$V_{SD}$	--	--	1.1	V
Reverse Recovery Time	$I_S = 17\text{A},$	$t_{rr}$	--	32.5	--	ns
Reverse Recovery Charge	$di/dt = 100\text{A}/\mu\text{s}$	$Q_{rr}$	--	21.6	--	nC

**Notes:**

- Package current limit.
- $L = 0.3\text{mH}, V_{GS} = 10\text{V}, R_G = 25\Omega,$  Starting  $T_J = 25^\circ\text{C}.$
- Pulse test: Pulse Width  $\leq 300\mu\text{s},$  duty cycle  $\leq 2\%.$
- Switching time is essentially independent of operating temperature.

**ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TQM056NH04LCR RLG	PDFN56U	2,500pcs / 13" Reel
TQM056NH04LCR-V RLG	PDFN56U	2,500pcs / 13" Reel

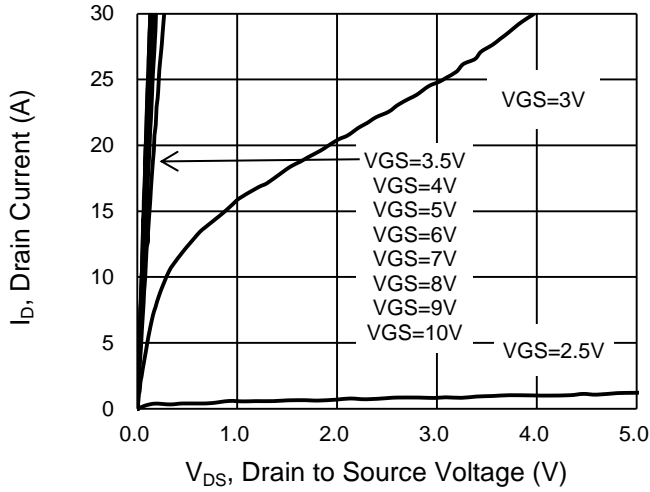
**Notes:**

V : HOT test

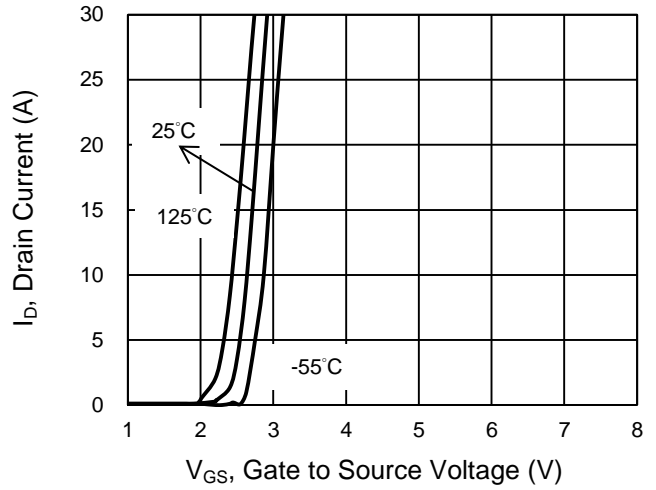
**CHARACTERISTICS CURVES**

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

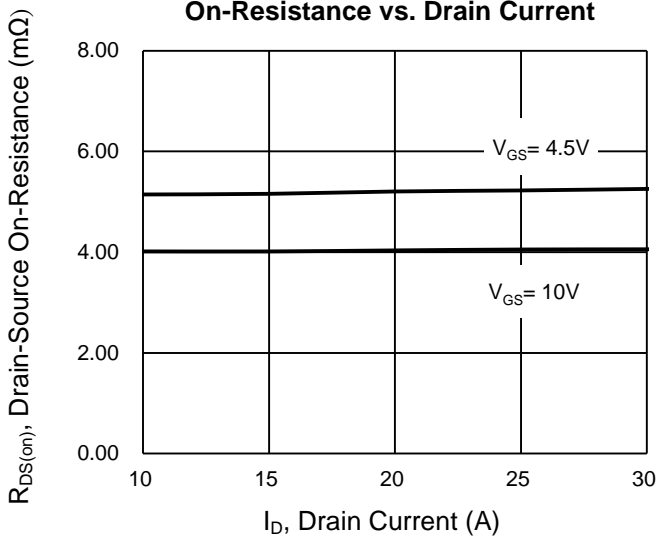
**Output Characteristics**



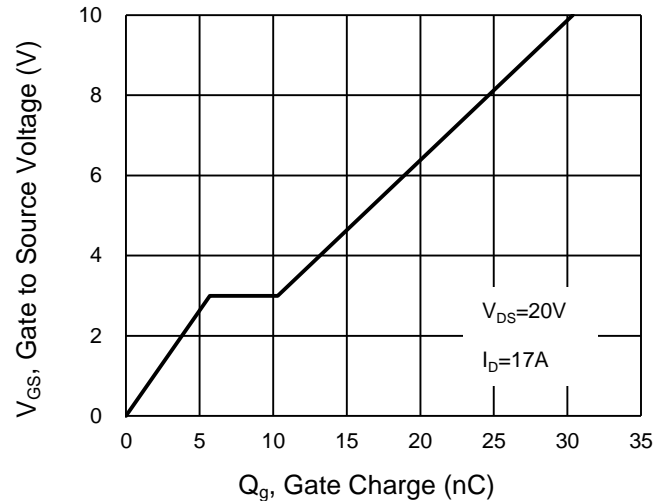
**Transfer Characteristics**



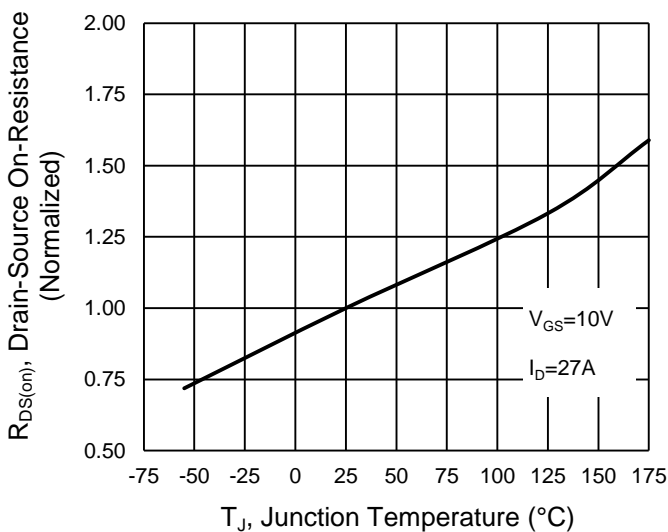
**On-Resistance vs. Drain Current**



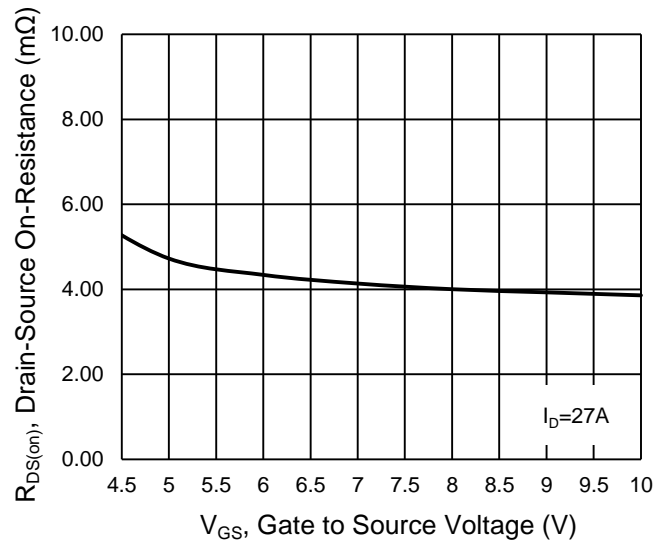
**Gate-Source Voltage vs. Gate Charge**



**On-Resistance vs. Junction Temperature**

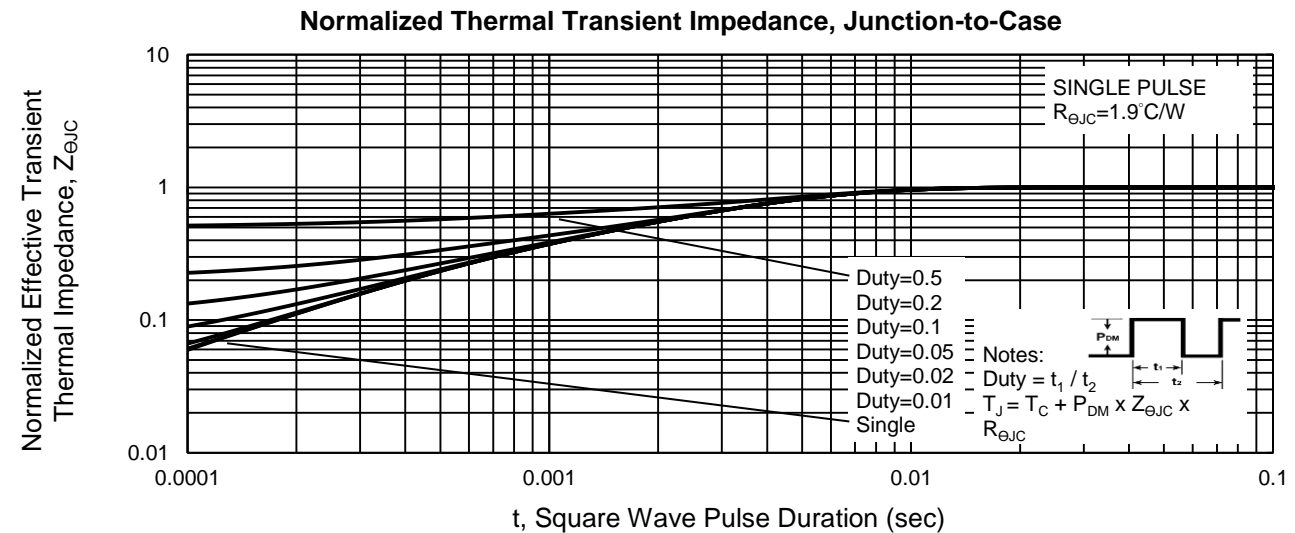
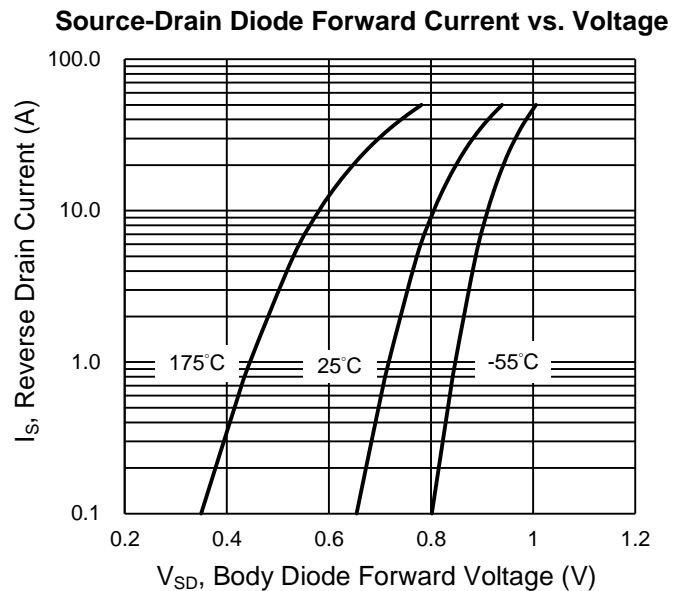
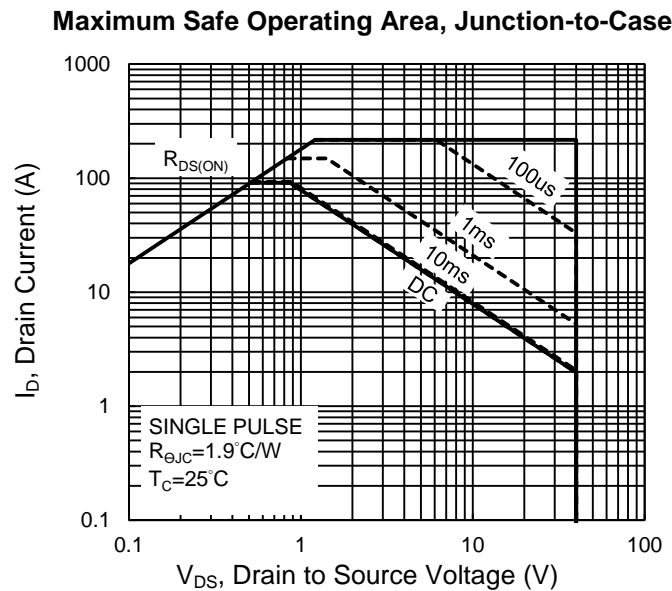
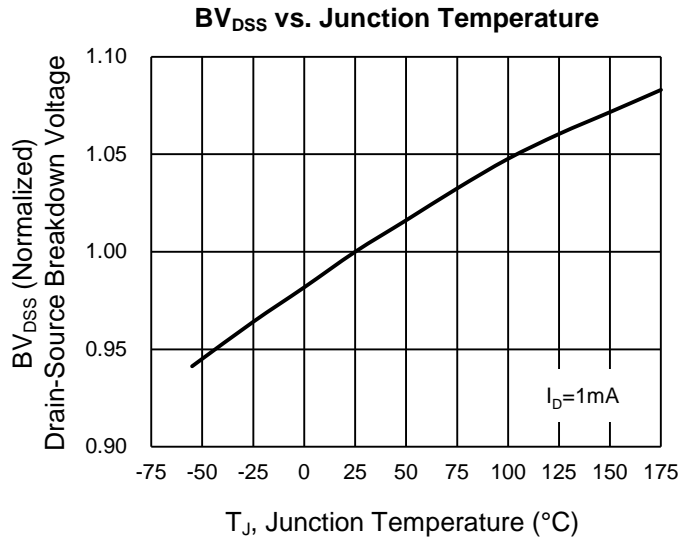
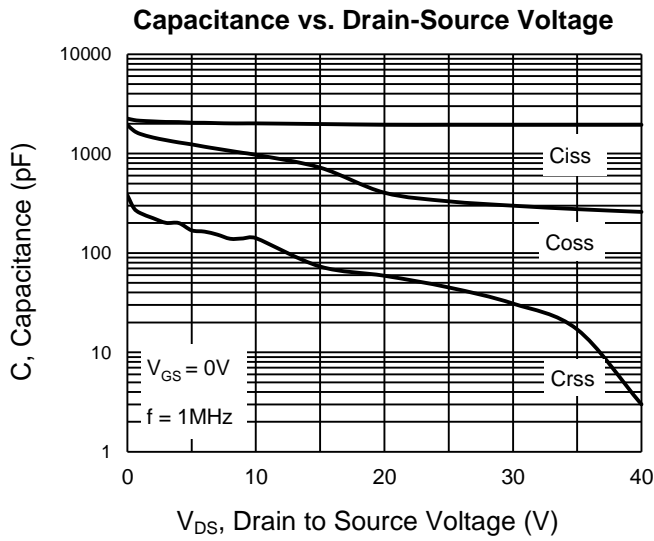


**On-Resistance vs. Gate-Source Voltage**



**CHARACTERISTICS CURVES**

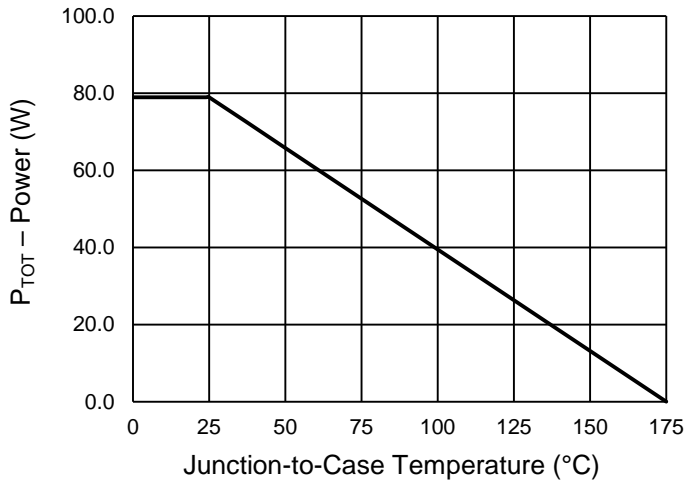
( $T_A = 25^\circ\text{C}$  unless otherwise noted)



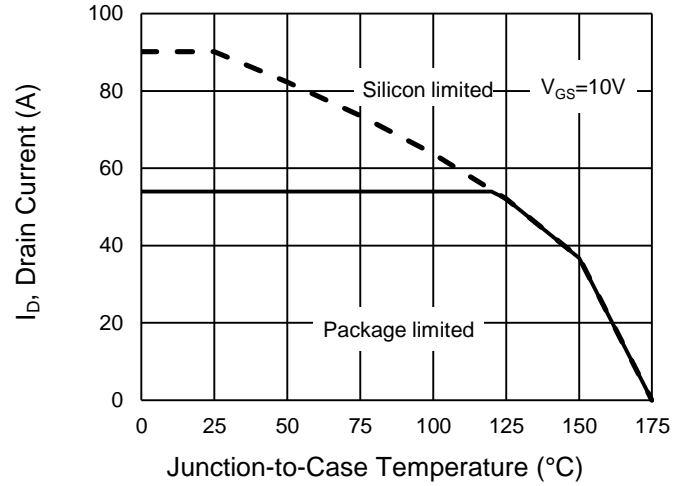
**CHARACTERISTICS CURVES**

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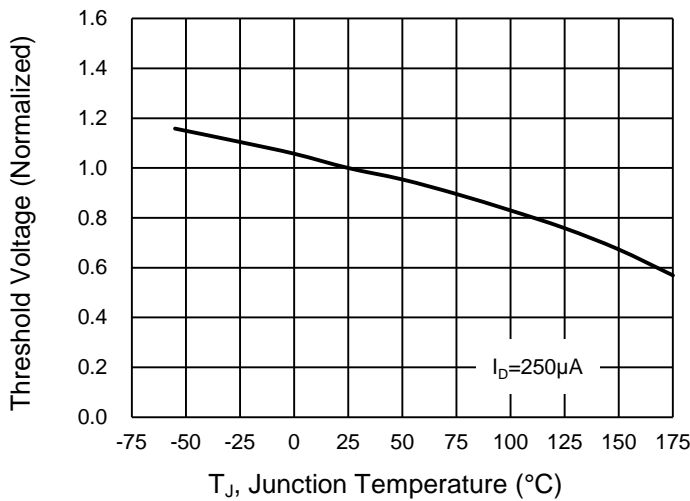
**Power Dissipation**



**Drain Current**

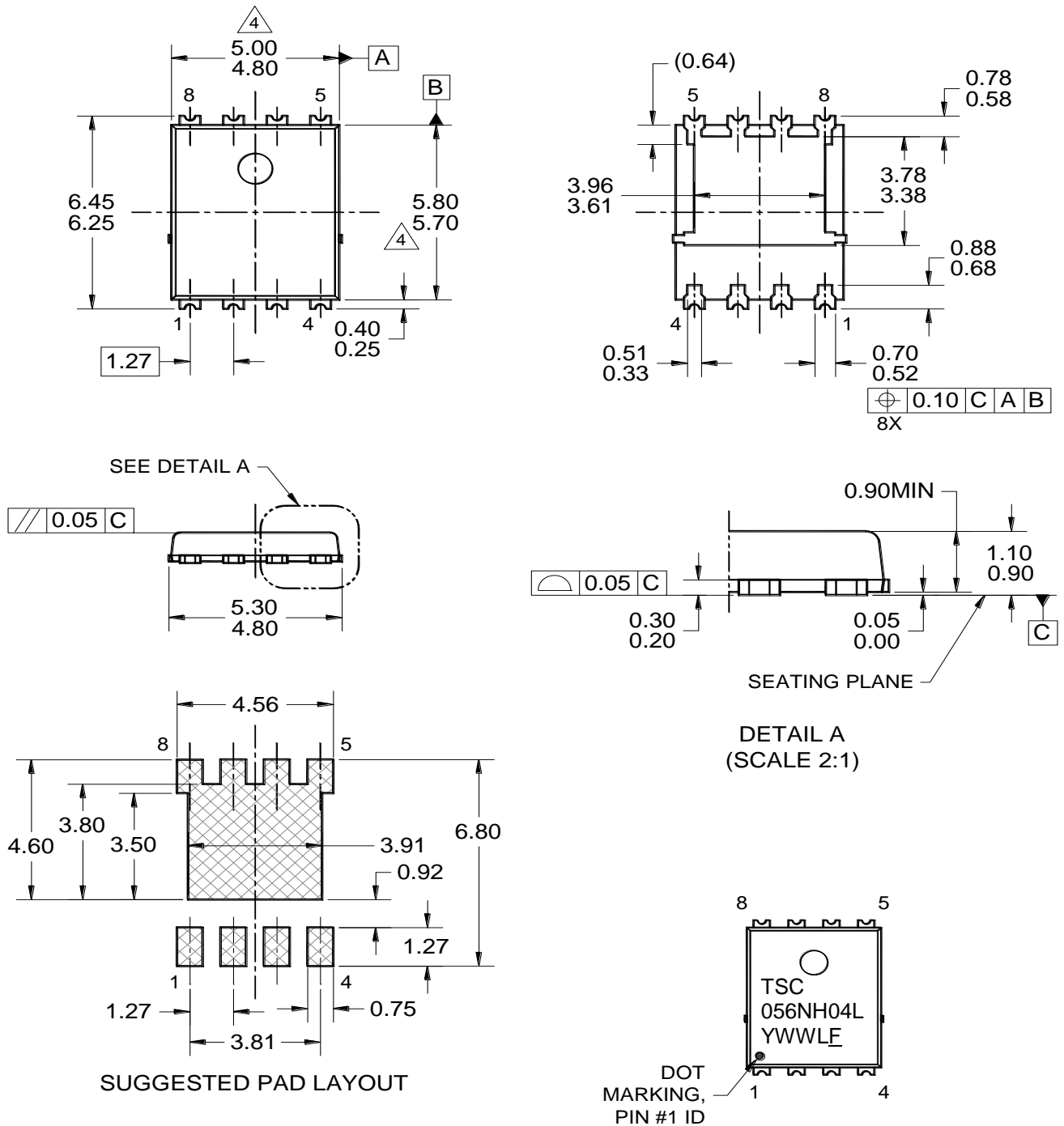


**Normalized gate threshold voltage vs Temperature**



**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)

PDFN56U



**NOTES: UNLESS OTHERWISE SPECIFIED**

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEITA ED-7500B, EIAJ SC-111BB.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-PDFN56U-023 REV A.

**MARKING DIAGRAM**

- P/N = MARKING CODE  
 Y = YEAR CODE  
 WW = WEEK CODE (01~52)  
 L = LOT CODE (1~9, A~Z)  
 F = FACTORY CODE  
 - = AEC-Q101 QUALIFIED

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