Digital controller for STC/HSTC topologies

Features

- Digital controller for STC/HSTC topologies
- Support wide conversion ratio from 2:1 to 10:1 to provide several Vout
- State Machine Event Driven (SMED) to implement key control features:
  - Current limit in combination with Hot swap controller
  - Operating input voltage window
  - Conversion ratio control
  - PWM frequency and deadtime management to guarantee ZCD function
  - Soft-start control
  - Driver management
  - Temperature control
- Typical application: Server DC/DC intermediate bus generation from 40 V to 60 V input voltage, 200 W to 2 kW output power range
- Peripherals
  - 10-bit ADC
  - UART interface
  - I^2C master fast/slow speed rate
  - GPIOs
- Memory
  - Flash and EEPROM with read-while-write (RWW) and Error Correction Code (ECC)
  - Program memory: 32 Kbytes Flash; data retention: 20 years at 55 °C after 1000 cycles at 55 °C
  - Data memory: 1 Kbyte true data EEPROM; data retention: 20 years at 55°C after 1000 cycles at 85 °C
  - RAM: 6 Kbytes
- Operating temperature: -40 °C up to 105 °C
- Package: VFQFPN32 5x5 mm

Product status link
STNRG328S

Product label
SUSTAINABLE TECHNOLOGY

Description

The STNRG328S is a digital controller for STC/HSTC open loop resonant converter from STMicroelectronics. It performs a power conversion from an input voltage in a typical range of 40 V to 60 V to an output voltage with a programmable conversion ratio from 2:1 to 10:1 with fixed duty cycle and programmable frequency from 140 kHz to 300 kHz.

It's able to deliver an output power in the range from 500 W up to 2 KW with very high efficiency in wide load range and with efficiency peak of 98.4% .

A State Machine Event Driven (SMED) implements the control strategy to ensure all the STC/HSTC control functions, in particular the ZCD (Zero Current Detection) feature allows a management of the deadtime and the switching frequency in order to achieve the perfect LC resonance and top efficiency independently from the external component variations.

The STNRG328S firmware is specifically designed to program the SMED and implement the control strategy.

1 STC typical application

Figure 1 shows a typical STC application for 4:1 conversion ratio. The STNRG328S works in companion with STPRDC02A gate drivers designed for STC applications, and a hot-swap circuit (typically an e-fuse) to avoid damages during hot plug-in of the input 48 V bus.

Figure 1. STC typical application
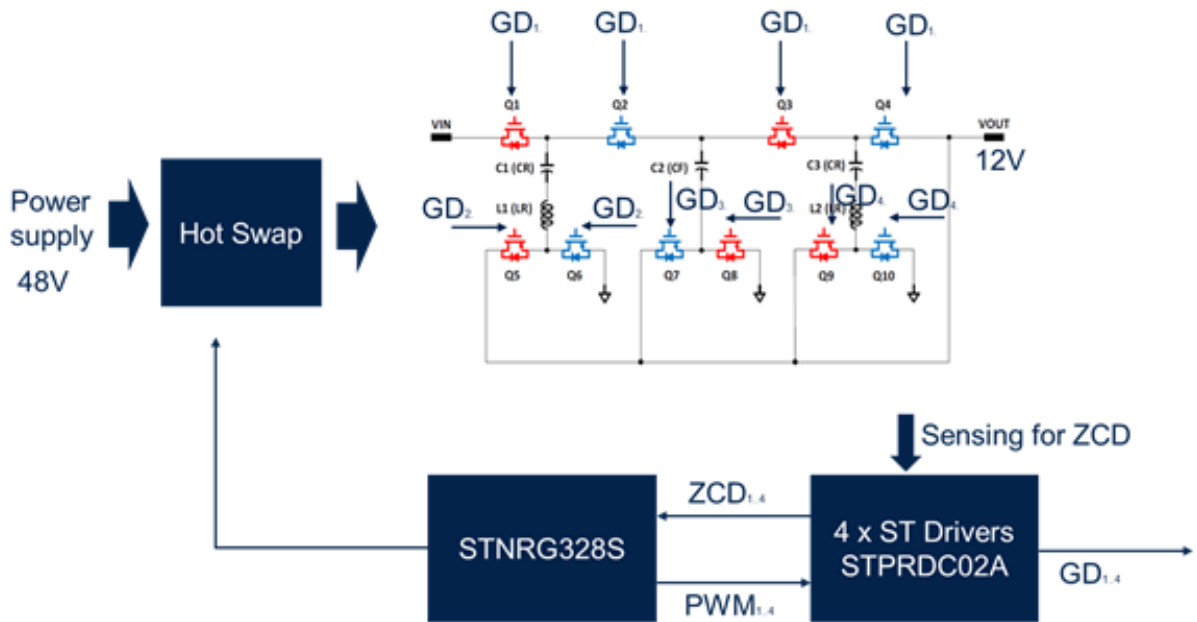
2 STNRG328S system architecture

The core of the STNRG328S is the SMED (State Machine Event Driven) which allows the device to generate six independent PWMs and can be programmed to react to internal and external events and may evolve without any software intervention. The SMED is configured with a CPU supervisor that is an STM8 microcontroller with the support of E^2PROM, Flash and RAM memories for data and code program storing.

A specific STMicroelectronics proprietary firmware is designed to configure the SMED to fit the STC/HSTC applications.

The Communication and the monitoring is supported with multifunctional bidirectional GPIO with highly robust design, immune against current injection and fast digital input DIGIN, with configurable pull-up, UART asynchronous with SW flow controls and bootloader support and I^2C master/slave fast/slow speed rate and a sequential ADC which can be configured to continuously sample up to 6 channels.

The STNRG328S is complete with power management to ensure several low modes power to maximize the efficiency and a full set of protections for secure reading and writing register access and against overtemperature.

Internal PLL provides 96 MHz clock for high frequency operations and to generate accurate PWMs.

The IC can be supplied both with 5 V and 3.3 V

Figure 2 shows STNRG328S device architecture.

Figure 2. STNRG328S device architecture
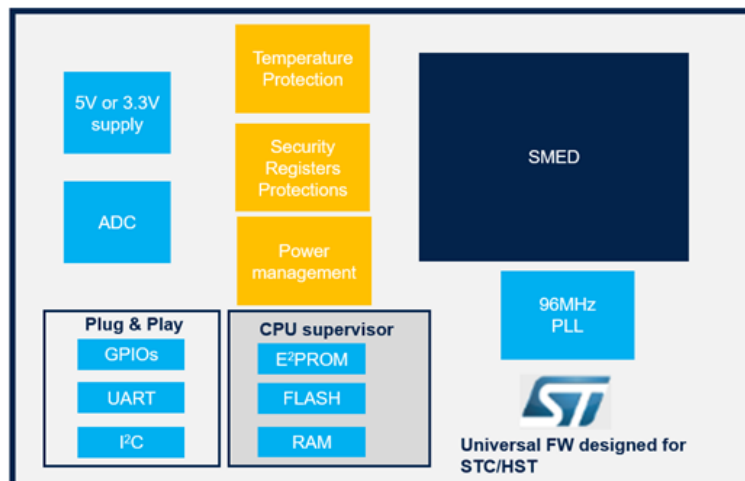
2.1 Firmware

The STNRG328S is provided with a turnkey software package distributed as a binary file to configure the SMED to fit STC/HSTC topologies in the whole range of conversion ratios.

The STNRG328S provides PMBUS Communication interface, for external programming of parameters and STC/HSTC control.

The firmware architecture includes the following functions:

- Main control
- SMED initialization
- PMBUS
- ZCD matrix
- Utility spec.
- E^2PROM
- LIB
- Interrupt

Main control manages the states through which the event machine passes during switching activity or on steady mode. This section controls also the PWMs frequency, checks the fault conditions, triggers the protections and initializes the peripherals of the device.

SMED initialization is the part that sets the initial conditions for the states in order to have initial PWMs frequency and deadtimes ready after the start-up.

PMBUS initializes communication on I^{2}C and handles the command for reading and writing formatted according to PMBUS protocol.

ZCD matrix defines in the RAM&E^{2}PROM the frequencies and deadtimes used in ZCD board configuration and depending on the input voltage. Then it also defines the functions of writing, reading and searching in ZCD tables.

Utility spec. implements the software requests depending on the switching type selected.

**E^{2}PROM** defines the programmable parameters and structures stored in NVM.

LIB contains the variables to access the registers of the device.

Interrupt schedules the ADC sequence and processes the relative operations, sets the timeout of each system state and reports an error on I^{2}C in case of error, collects 7 samples for each ADC conversion sequence, handles the data bytes of PMBUS command from/to I^{2}C, detects if the pin ENABLES is high or low to turn on or off the device, detects the events corresponding to undervoltage condition, Vdrive undervoltage and overvoltage condition.

3 STNRG328S pinout and pin description

This section shows the pinout used by the STNRG328S.

Figure 3. STNRG328S pinout
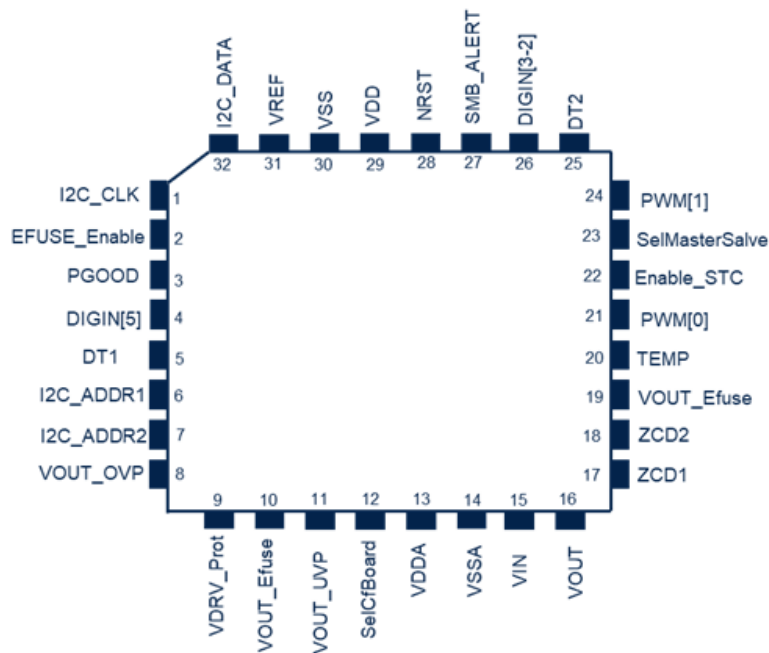
Table 1. Pinout description

Pin number	Pin name	Pin type	Description
1	I2C_CLK	General purpose I/O	Clock signal of I^{2}C bus
2	EFUSE_Enable	SMED channel PWM4	STNRG enables the EFUSE circuit
3	PGOOD	General purpose I/O	The pin shows if the STC is running
4	DIGIN[5]	Digital input	PWM0 signal as input of SMED2 (deadtime)
5	DT1	Digital output	Deadtime 1 signal (master or slave according to pin 23)
6	I2C_ADDR1	General purpose I/O	First bit of I^{2}C address selection and output for external mux management
7	I2C_ADDR2	General purpose I/O	Second bit of I^{2}C address selection
8	VOUT_OVP	Comparator positive input	Analog positive input comparator 3 for VOUT OVP protection based on VIN
9	VDRV_Prot	Comparator positive input	Analog positive input comparator 2 for Vdriver protection
10	VOUT_Efuse	Comparator negative input	Negative analog comparator input 3 for Output Efuse management
11	VOUT_UVP	Comparator positive input	Analog positive input comparator 1 for Vout UVP protection
12	SelCfgBoard	Comparator positive input	Analog positive input comparator 0, to select 15 available STC configurations
13	VDDA	Power supply	Analog power supply
14	VSSA	Power supply	Analog ground

Pin number	Pin name	Pin type	Description
15	VIN	Analog input	ADC input channel 5 for INPUT voltage reading
16	VOUT	Analog input	ADC input channel 4 for OUTPUT voltage reading
17	ZCD1	Analog input	ADC input channel 3 for ZCD1 management
18	ZCD2	Analog input	ADC input channel 2 for ZCD2 management
19	VOUT_Efuse	Analog input	ADC input channel 1 for Efuse Output reading
20	TEMP	Analog input	ADC input channel 0 for external Temp reading set by NTC resistor
21	PWM[0]	Digital output	PMW X square wave at resonant switching frequency, fixed 50% duty
22	Enable_STC	Digital input	The pin's level enables (High) or disables (Low) the STC device
23	SelMasterSlave	Digital input	The pin select ZCD logic for master/slave configuration on the two resonant paths
24	PWMY[1]	Digital output	Complementary of PWMX[0] signal
25	DT2	Digital output	Deadtime 2 signal (master or slave according to pin 23)
26	DIGIN[3_2]	Digital input	PWM0 signal as input of SMED2 (deadtime)
27	SMB_ALERT	Analog output	The pin reports if there has been a failure or there is a SWIM input to program STC
28	NRST	General purpose I/O	Reset
29	VDD	Power supply	Digital and I/O power supply
30	VSS	Power supply	Digital and I/O ground
31	VREF	Power supply	Reference 1.8 V regulator capacitor
32	I2C_DATA	General purpose I/O	Data signal of I^{2}C bus

Note: The operative voltage of Analog Input pins ranges from 0 V to 1.2 V.

4 Pins functional description

This section describes the functions related to the pins of the device. For more information refer to the reference design STC Application Note.

4.1 Power supplies

The digital portion of the STNRG328S is powered using VDD & VSS (typically 3.3 V in STC application).

The analog portion of the STNRG328S is powered using VDDA & VSSA (typically 3.3 V in STC application).

VDD & VDDA should be correctly filtered to allow correct operation of device.

The STNRG328S generates its own internal power supply which needs a filter LC, L (pn: WE 74279262) capacitor of 1 µF on VOUT pin.

4.2 EFUSE_Enable

This pin is controlled by the SMED PWM4 channel output. In normal condition the level is high and the EFUSE circuit is active. When the protections are triggered the pin's level is set low and the EFUSE circuit is disabled.

4.3 PGOOD

The pin is configured as open-drain output. Pgood rises at the end of the soft-start with few mS of delay. The high level indicates that STC is ON and the output voltage is regulated. The low level indicates that the STC is OFF.

4.4 DIGIN[5], DIGIN[3_2]

Pins 4 and 26 are configured as digital input. They are connected to output of PWM0 channel and used as input of state machine of SMED2/3 to generate the deadtime signals on pins DT1 and DT2.

4.5 I2C_ADDR1, I2C_ADDR2

These pins are configured as analog input with internal pull-up and are used to select the specific I^2C address of the device.

The possible combinations are four:

Table 2. Configurations of pins 6 and 7

Pin6	Pin7	Address	7bit Address
GND	GND	0xA0	0x50
Open	GND	0xA4	0x52
GND	Open	0xA8	0x54
Open	Open	0xAC	0x56

Pin 6, after the setup of I^2C address, is configured as an analog output in push-pull mode to drive the mux for the double temperature reading.

4.6 VOUT_OVP, VDRV_Prot, VOUT_UVP, VOUT_Efuse

The pin *VDRV_Prot* detects a dangerous lower level of MOSFET gate supply; pin 11 and pin 8 detect UVP (Undervoltage Protection) and OVP (Overvoltage protection), while *VOUT_Efuse* helps to detect EFuse / Hot swap to manage the Overcurrent protection .

These signals are used by the SMED state machine to trigger the protection (lowering ENABLE_EFUSE pin) if an anomaly occurs.

The VOUT_UVP (pin 11) is the positive input of the comparator 1 (see *Section 7)*, the negative input level of comparator 1 is set by a software table which level is adjusted automatically when the Vin changes. Output voltage of unregulated solution varies with the input voltage and a tracking software implementation has been adopted.

Considering the new fast input variation on server application, Vin tracking is clamped up to the min. voltage, allowing a fast swing of input signal relaxing the UVP protection threshold.

4.7 SelCfgBoard

This pin selects in the software the board configuration corresponding to level voltage of the resistor divider connected to the pin.

The board configurations are:

Table 3. Boards configurations

Config.	Board	Ratio	V_CPP0	Freq. SW (kHz)	Freq. min. (kHz)	Freq. max. (kHz)	Cap.
0	STC	4:1	41 mV	ZCD	-	-	X7R
1	STC	3:1	123 mV	ZCD	-	-	X7R
2	STC	2:1	205 mV	ZCD	-	-	X7R
3	STC	2:1	287 mV	**330**	**330**	**330**	U2J
4	STC	2:1	369 mV	**360**	**360**	**360**	U2J
5	STC	3:1	451 mV	**330**	**330**	**330**	U2J
6	STC	4:1	533 mV	**330**	**330**	**330**	U2J
7	STC	4:1	615 mV	**360**	**360**	**360**	U2J
8	STC	4:1	697 mV	**390**	**390**	**390**	U2J
9	HSTC	4:1	779 mV	**180**	**180**	**180**	U2J
10	HSTC	5:1	861 mV	**200**	**200**	**200**	U2J
11	HSTC	5:1	943 mV	**500**	**500**	**500**	U2J
12	HSTC	6:1	1025 mV	**180**	**180**	**180**	U2J
13	HSTC	8:1	1107 mV	**180**	**180**	**180**	U2J
14	HSTC	10:1	1189 mV	**180**	**180**	**180**	U2J

4.8 ADC channel inputs

The ADCINx (x=0,1,2,3,4,5) input channels are used for sampling the following analog signals:

- TEMP : ADCIN[0] converts the signal of NTC (NTCS0603E3104JXT) to get the temperature.
- VOUT_Efuse : sampled by ADCIN[1] for the soft-start and OCP.
- ZCD2 : by ADCIN[2] monitors the signal coming from the driver that detects circulating current on the MOSFET's diode parasitic to update the frequency or deadtime (according to master/slave configuration set by pin 23 (DIGIN1)) in the ZCD algorithm.
- ZCD1 : by ADCIN[3] monitors the signal coming from the driver that detects circulating current on the MOSFET's diode parasitic to update the frequency or deadtime (according as to master/slave configuration set by pin 23 (DIGIN1)) in the ZCD algorithm.
- VOUT : ADCIN[4] samples the output voltage .
- VIN : ADCIN[5] samples STC input voltage.

4.9 SelMasterSlave

Pin 23 as DIGIN[1] is to be used to select the master/slave. The selected configurations are:

Table 4. Master/slave configuration

DIGIN[1]	Master	Slave	Configuration value
Low level	STM1 (ADC2, PWM2)	STM2 (ADC3, PWM3)	1
High level	STM2 (ADC3, PWM3)	STM1 (ADC2, PWM2)	2

4.10 SMB_ALERT

Pin 27 is configured as GPIO analog output in open-drain mode. If asserted, the pin indicates that a failure has triggered.

4.11 PMBUS Protocol

The embedded firmware in the STNRG328S supports the PMBUS communication protocol.

The Power Management Bus ("PMBus") is an open standard protocol that defines a means of communicating with power conversion and other devices.

For more information, please see the System Management Interface Forum website www.powerSIG.org.

The PMBUS is based on the standard I^2C communication protocol. It is possible to poll the device (slave) using an I^2C host (master to send/receive PMBUS commands) connected to the I^2C data&clock pins of the device.

The supported PMBUS commands are listed in Table 5:

Table 5. PMBUS ommands

PMBUS command	Code	Operation type	Size (byte)	Comment
PMBUS_ON_OFF_CONFIG	0x02	R/W	1	Turn off/on STC (*)
PMBUS_CLEAR_FAULTS	0x03	W	1	Clear the internal status registers
PMBUS_WRITE_PROTECT	0x10	R/W	1	Enable/disable the write protection of EEPROM
PMBUS_CAPABILITY	0x19	R	1	The command returns the key capabilities of the PMBUS device
PMBUS_SMBALERT_MASK	0x1B	W	2	The command sets the mask of its status command to enable/disable the SMB_ALERT pin. The first data byte is the PMBUS code of the command, the second data byte is the mask. By default the mask is zero, that is, it means that the SMB_ALERT pin is raised when there is a fault for Vin, Vout, Temp, etc.
PMBUS_VOUT_MODE	0x20	R/W	2	Read/write ok. Not implemented functionality.
PMBUS_VIN_ON	0x35	R/W	2	Set/get the input voltage beyond STC turn-on
PMBUS_VIN_OFF	0x36	R/W	2	Set/get Vin_off which intervenes when an undervoltage occurs, the STC goes into the UVLO state but is still on, if it remains there for a certain time then it goes into the shutdown state
PMBUS_VIN_OV_FAULT_LIMIT	0x55	R/W	2	Set/get the input voltage that causes an input overvoltage
PMBUS_STATUS_BYTE	0x78	R/W	1	The commands returns one byte of information with a summary of the most critical faults and clears specific bit

PMBUS command	Code	Operation type	Size (byte)	Comment
PMBUS_STATUS_WORD	0x79	R/W	2	The command returns two bytes of information with a summary of the unit's fault condition and clears specific bit
PMBUS_STATUS_VOUT	0x7A	R/W	1	The command returns the info about the Vout fault cause
PMBUS_STATUS_INPUT	0x7C	R/W	1	The command returns the info about the Vin and Iin and clears specific fault's bit
PMBUS_STATUS_TEMPERATURE	0x7D	R/W	1	The command returns the info about the temperature and clears specific fault's bit.fault&warning and clears specific fault's bit
PMBUS_STATUS_CML	0x7E	R/W	1	The command returns the general conditions of the faults and clears specific fault's bit
PMBUS_STATUS_OTHER	0x7F	R/W	1	*TBD*
PMBUS_STATUS_MFR_SPECIFIC	0x80	R/W	1	The command detects the Undervoltage condition on Vdrive rising the flag to 1
PMBUS_READ_VIN	0x88	R	2	The command returns the input voltage in the LINEAR11 numeric format
PMBUS_READ_VOUT	0x8B	R	2	The command returns the output voltage in ULINEAR16 (?) numeric format
PMBUS_READ_TEMPERATURE_1	0x8D	R	2	The command returns temperature read from the device. Two bytes are encoded in LINEAR11 numeric format.
PMBUS_READ_TEMPERATURE_2	0x8E	R	2	The command returns temperature read from the device. Two bytes are encoded in LINEAR11 numeric format. If there is only temperature sensor on the board, the returned value is 0x00.
PMBUS_READ_FREQUENCY	0x95	R	2	The command returns the switching frequency of the PMBus device. The two bytes are encoded in the numeric format LINEAR11.
PMBUS_PMBUS_REVISION	0x98	R	5	The command reads the manufacturer's revision
PMBUS_MFR_MODEL	0x9A	R	10	The command reads the manufacturer's model number
PMBUS_MFR_REVISION	0x9B	R	5	The command gets the firmware revision
PMBUS_MFR_DATE	0x9D	R	5	The command reads the date the device was manufactured
PMBUS_MRF_MAX_TEMP_1	0xC0	R/W	2	The command sets/gets the 1st max. rated temperature of the manufacturer. Unit is degree Celsius.
PMBUS_MRF_MAX_TEMP_2	0xC1	R/W	2	The command sets/gets the 2nd max. rated temperature of the manufacturer. Unit is degree Celsius.
PMBUS_MFR_SPECIFIC_12	0xD0	R/W	2	MFR_WAIT_EN_FAULT: Set/Get the number of system ticks before enabling faults, after entering ST_ON
PMBUS_MFR_SPECIFIC_13	0xD1	R/W	2	MFR_WAIT_EN_FAULT1: Set/Get the number of system ticks before enabling faults, after entering ST_ON (second restart)
PMBUS_MFR_SPECIFIC_14	0xD2	R/W	2	MFR_WAIT_TIMEPWRUP: Read/write the number of ticks to wait at power-up
PMBUS_MFR_SPECIFIC_15	0xD3	R/W	2	MFR_WAIT_BEFORE_EFUSE: Read/write the number of ticks to wait before ENEF use asserted

PMBUS command	Code	Operation type	Size (byte)	Comment
PMBUS_MFR_SPECIFIC_17	0xD5	R/W	2	MFR_VOUT_EFUSE_MIN: Set/get minimum value of Vout Efuse for which Vout Efuse undervoltage is triggered
PMBUS_MFR_SPECIFIC_18	0xD6	R/W	2	MFR_OCP_VALUEDIF: Voltage difference between input voltage and Vout Efuse to detect an Overcurrent condition
PMBUS_MFR_SPECIFIC_19	0xD7	R	2	Read conversion ratio
PMBUS_MFR_SPECIFIC_20	0xD8	-	-	Not implemented
PMBUS_MFR_SPECIFIC_21	0xD9	R/W	2	MFR_ VDRIVER_UVP_DAC: Set/get the internal reference for undervoltage for Vdriver. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_22	0xDA	R/W	2	MFR_VIN_SHUTDOWN: Set/get Input voltage threshold. When the input voltage becomes less than this value, the STC is put in OFF state. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_23	0xDB	R/W	2	MFR_SWITCHFREQ_FF_STEP: Set/get the step of the switching frequency. At feed forward threshold, switching frequency changes by this value (kHz), put this value into SWITCHFREQ_FF_STEP. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_24	0xDC	R/W	2	MFR_FF_THRESHOLD_VMIN: Set/get the Feed forward frequency step threshold (min. voltage) put this value into FF_THRESHOLD_VMIN. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_25	0xDD	R/W	2	MFR_FF_THRESHOLD_VMAX: Set/get Feed forward frequency step threshold (max. voltage) put this value into FF_THRESHOLD_VMAX. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_26	0xDE	R/W	2	MFR_ENABLE_BOOTLOADER: Enable/disable bootloader by UART
PMBUS_MFR_SPECIFIC_27	0xDF	R/W	2	MFR_SWITCH_FREQ: Set/get the Programmable switching frequency. Numeric format is LINEAR11.
PMBUS_MFR_SPECIFIC_28	0xE0	R/W	2	MFR_OVP_COUNTER: Set/get the number of OVP faults
PMBUS_MFR_SPECIFIC_29	0xE1	R/W	2	MFR_UVP_COUNTER: Set/get the number of UVP faults
PMBUS_MFR_SPECIFIC_30	0xE2	R/W	2	MFR_OCP_COUNTER: Set/get the number of OCP faults
PMBUS_MFR_SPECIFIC_31	0xE3	R/W	2	MFR_THERMSHDW_COUNTER: Set/get the number of thermal shutdown faults
PMBUS_MFR_SPECIFIC_32	0xE4	R/W	6	MFR_LOCK: Insert password (6 bytes) to lock EEPROM writing
PMBUS_MFR_SPECIFIC_33	0xE5	R/W	6	MFR_UNLOCK: Insert password (6 bytes) to unlock EEPROM writing
PMBUS_MFR_SPECIFIC_34	0xE6	-	-	MFR_ PWMFREQMIN: NOT IMPLEMENTED
PMBUS_MFR_SPECIFIC_35	0xE7	-	-	MFR_ PWMFREQMAX: NOT IMPLEMENTED
PMBUS_MFR_SPECIFIC_36	0xE8	2	R/W	Return the count of Vout_Efuse falis
PMBUS_MFR_SPECIFIC_38	0xEA	1	R	MFR_START_CRC_CHECK: Start the CRC check
PMBUS_MFR_SPECIFIC_39	0xEB	4	R	MFR_GET_CRC_RESULT: Get the CODE CRC result
PMBUS_MFR_SPECIFIC_40	0xEC	2	R	MFR_GET_EEPROM_CHECKSUM: Get the EEPROM checksum

PMBUS command	Code	Operation type	Size (byte)	Comment
PMBUS_MFR_SPECIFIC_44	0xF0	4	R	MFR_GRT_DATA_CRC_RESULT: Get the DATA CRC result
PMBUS_MFR_SPECIFIC_47	0xF3	2	R/W	Set/Get VOUT_SETUPSWITCH
PMBUS_USER_DATA_00	0xB0	1	R/W	Get/set the index of ZCD Matrix table. The range is [0,18], outside of this range the command returns the error code 0xFF.
PMBUS_MFR_SPECIFIC_45	0xF1	8	R/W	Read/write the ZCD parameters in the ZCD Matrix table (RAM if STC is ON, EEPROM if STC is OFF) at the index specified by the command. If the index is out of range, the command returns the sequence of error code 0xFF.
PMBUS_MFR_SPECIFIC_46	0xF2	1	R/W	The command loads the ZCD Matrix table from RAM to FLASH. It returns 1 if the copy is successful, otherwise it returns 0.
PMBUS_MFR_SPECIFIC_41	0xED	1	R/W	The command reads/writes the increment of SMED0 clock from/to FLASH memory. The range is [0,50]. The command returns 0xFF when the value is out of the range or when the STC is ON.
PMBUS_USER_DATA_01	0xB1	9	R	The command returns the current line and the relative index of the ZCD Matrix, corresponding to Vin applied when STC is ON. If STC is OFF the bytes are 0xFF
PMBUS_USER_DATA_02	0xB2	1	R	Read the configuration master/slave
PMBUS_USER_DATA_03	0xB3	1	R	Return the board configuration
PMBUS_USER_DATA_04	0xB4	1	R	Return the Trim Byte (it indicates that the test EWS1, WS2, Final are passed)

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to VSS. VDDA and VDD must be connected to the same voltage value. VSS and VSSA must be connected together with the shortest wire loop.

5.2 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at TA = 25 °C and TA = TA max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.3 Typical values

Unless otherwise specified, typical data are based on TA = 25 °C, VDD and VDDA = 5 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

5.4 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

5.5 Typical current consumption

For typical current consumption measurements, VDD and VDDA are connected together as shown in Figure 4.

Figure 4. **Supply current measurement conditions**
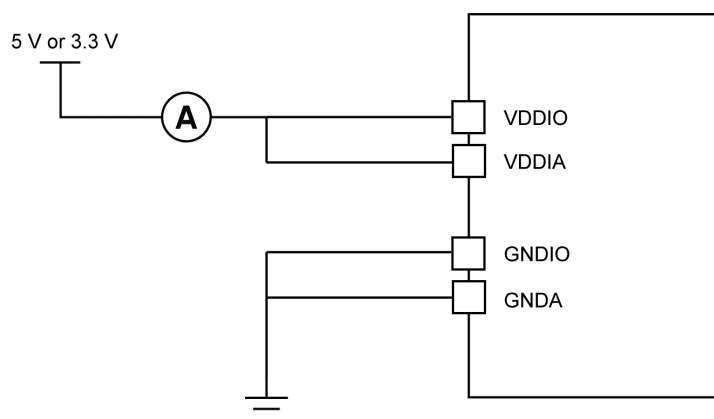
5.6 Loading capacitors

The loading conditions used for pin parameter measurement are shown in Figure 5.

Figure 5. Pin loading conditions

50 pF
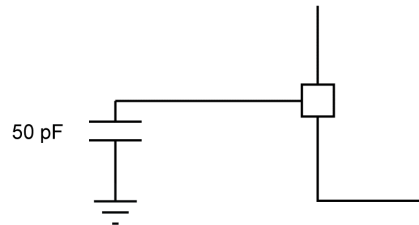
GIPD090520131536FSR

5.7 Pin output voltage

The input voltage measurement on a pin is described in Figure 6.

Figure 6. Pin Input voltage

V_{IN}
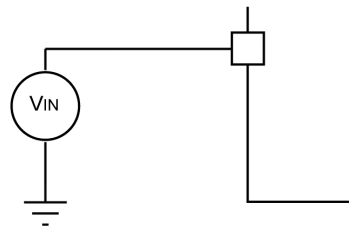
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5.8 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
$V_{DDX} - V_{SSX}$	Supply voltage[1]	-0.3	6.5	V
V_{IN}	Input voltage on any other pin[2]	V_{SS}-0.3	V_{DD}+0.3	
$V_{DD} - V_{DDA}$	Variation between different power pins		50	mV
$V_{SS} - V_{SSA}$	Variation between all the different ground pins[3]		50	mV
$V_{ESD(HBM)}$	Human Body Model TA = 25 °C, conforming to JEDEC/JESD22-A114E		2000	V
$V_{ESD(CDM)}$	Charge Device Model TA = 25 °C, conforming to ANSI/ESD STM 5.3.1 ESDA		500	V
$V_{ESD(MM)}$	Machine Model TA = 25 °C, conforming to JEDEC/JESD-A115-A		200	V

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS},V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 7. Current characteristics

Symbol	Ratings	Max.[1]	Unit
I_{VDDX}	Total current into V_{DDX} power lines[2]	20 mA	mA
I_{VSSX}	Total current out of V_{SSX} power lines[2]	20 mA	
I_{IO}	Output current sunk by any I/Os and control pin	5 mA	
	Output current source by any I/Os and control pin	3 mA	
$I_{INJ(PIN)}$ [3][4]	Injected current on any pin	±4	
$I_{INJ(TOT)}$ [3][4][5]	Sum of injected currents	±20	

1. Data based on characterization results, not tested in production.
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS},V_{SSA}) pins must always be connected to the external power supply.
3. $II_{NJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $\sum_{SIINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\sum_{SIINJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

Symbol	Ratings	Max.	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

5.9 Operating conditions

The device must be used in operating conditions that comply with the parameters in Table 9. In addition, full account must be taken for all physical capacitor characteristics and tolerances.

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{CPU}	Internal CPU clock frequency	-40 ≤ TA ≤ 105 °C	0		16	MHz
V_{DD1}, V_{DDA1}	Operating voltages		3[1]	5	5.5[1]	
V_{DD}, V_{DDA}	Nominal operating voltages		3.3[1]	5	5[1]	V
V_{ref}	Core digital power supply			1.8[2]		
	Cvref: capacitance of external capacitor[3]	at 1 MHz	470		3300	nF
	ESR of external capacitor[2]		0.05		0.2	Ω
	ESL of external capacitor[2]				15	nH
Θ_{JA}[4]	FR4 multilayer PCB	VFQFPN32		26		°C/W
T_A	Ambient temperature	Pd = 100 mW	-40		105	°C

1. The external power supply can range from 3 V to 5.5 V although IC performances are optimized for power supply equal to 5 V.
2. Internal core power supply voltage.
3. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
4. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (_{TJmax}-T_A)/\Theta_{JA}$.

Table 10. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IT}+$	Power-on reset threshold		2.65	2.8	2.98[1]	V
$V_{IT}-$	Brownout reset threshold		2.58	2.73	2.88[1]	
$V_{HYS(BOR)}$	Brownout reset hysteresis			70		mV

1. VDD rise must be monotone. The slew rate should be between 2 uS/v and 1 s/V.

5.9.1 Vref external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{Vref} to the VREF pin. The Cvref is specified in Section 5.9 Operating conditions. Care should be taken to limit the series inductance to less than 15 nH.

Figure 7. External capacitor C_{VOUT}
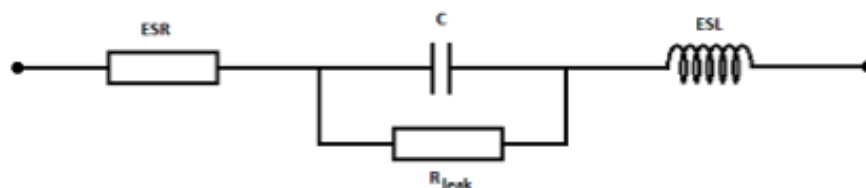
Note: *ESR is the equivalent series resistance and ESL is the equivalent inductance.*

5.9.2 Memory characteristics

Flash program and memory/data E^{2}PROM memory

General conditions: T_A = -40 °C to 105 °C.

Table 11. Flash program memory/data E^{2}PROM memory

Symbol	Parameter	Conditions	Min.[1]	Typ.[1]	Max.[1]	Unit
t$_{PROG}$	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	
t$_{ERASE}$	Erase time for 1 block (128 bytes)			3	3.3	ms
NWE	Erase/write cycles (program memory)[2]	T_A = 25 °C	10K			Cycles
	Erase/write cycles[2] (data memory)	T_A = 85 °C	100K			
		T_A = 105 °C	35K			
t$_{RET}$	Data retention (program memory) after 10K erase/write cycles at TA = 25°C	T_{RET} = 85 °C	15			Years
	Data retention (program memory) after 10K erase/write cycles at TA = 25°C	T_{RET} = 105 °C	11			
	Data retention (data memory) after 100K erase/write cycles at TA = 85°C	T_{RET} = 85 °C	15			
	Data retention (data memory) after 35K erase/write cycles at TA = 105°C	T_{RET} = 105 °C	6			
I$_{DDPRG}$	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC		2		mA

1. *Data based on characterization results, not tested in production.*
2. *The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.*

5.9.3 I/O port pin characteristics

The I/O port pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 12. Voltage DC characteristics

Symbol	Description	Min.[1]	Typ.	Max.[1]	Unit
V$_{IL}$	Input low voltage	-0.3		0.3 * V_{DD}	V
V$_{IH}$	Input high voltage[2]	0.7 * VDD		V_{DD}	
V$_{OL1}$	Output low voltage @ 3.3 V[3]			0.4[4]	
V$_{OL2}$	Output low voltage @ 5 V [3]			0.5	
V$_{OL3}$	Output low voltage high sink @ 3.3 V / 5 V[2] [5]		0.6[4]		
V$_{OH1}$	Output high voltage @ 3.3 V[3]	V_{DD}-0.4[4]			
V$_{OH2}$	Output high voltage @ 5 V[3]	V_{DD}-0.5			

Symbol	Description	Min.[1]	Typ.	Max.[1]	Unit
V_{OH3}	Output high voltage high sink @ 3.3 V / 5 V [2][5]	V_{DD}-0.6[4]			V
H_{VS}	Hysteresis input voltage[6]		0.1 * V_{DD}		
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. *Data based on characterization result, not tested in production.*
2. *Input signals cannot exceed V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).*
3. *Parameter applicable to signals: EFUSE_ENABLE, DT1, I2C_ADDR2, PWM[0], PWM[1], DT2,I2C_DATA*
4. *Electrical threshold voltage not characterized at -40 ºC.*
5. *Parameter applicable to the signals: SMB_ALERT,ENABLE_STC*
6. *Applicable to any digital inputs.*

Table 13. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.[1]	Unit
I_{OL1}	Standard output low level current @ 3.3 V and V_{OL1}[2]			1.5	mA
I_{OL2}	Standard output low level current @ 5 V and V_{OL2}[2]			3	
I_{OLhs1}	High sink output low level current @ 3.3 V and V_{OL3}[3]			5	
I_{OLhs2}	High sink output low level current @ 5 V and V_{OL3}[3]			7.75	
I_{OH1}	Standard output high level current @ 3.3 V and V_{OH1}[2]			1.5	
I_{OH2}	Standard output high level current @ 5 V and V_{OLH2}[2]			3	
I_{OHhs1}	High sink output high level current @ 3.3 V and V_{OH3}[3]			5	
I_{OHhs2}	High sink output high level current @ 5 V and V_{OH3}[3]			7.75	
I_{LKg}	Input leakage current digital - analog V_{SS} ≤ V_{IN} ≤ V_{DD}[4]			± 1	µA
$I_{\_Inj}$	Injection current [6]			± 4	mA
$\Sigma I_{\_Inj}$	Total injection current (sum of all I/O and control pins)[5]			± 20	

1. *Data based on characterization result, not tested in production.*
2. *Parameter applicable to signals: EFUSE_ENABLE,DT1,I2C_ADDR2,PWM[0],PWM[1],DT2,I2C_DATA*
3. *Parameter applicable to the signals: SMB_ALERT,ENABLE_STC.*
4. *Applicable to any digital inputs.*
5. *The maximum value must never be exceeded.*
6. *The negative injection current on VIN, VOUT, ZCD1, ZCD2, VOUT_Efuse,TEMP,pins have to be avoided since it affects ADC conversion accuracy*

5.9.4 Typical output level curves

This section shows the typical output level curves measured on a single output pin for the three pad family present in the STNRG328S device.

5.9.4.1 *Standard pad*

This pad class is associated to the following pins:

PGOOD,DIGIN[5],I2C_ADDR1,I2C_ADDR2,SELMASTERSLAVE,SMB_ALERT,I2C_DATA, ENABLE_STC

Figure 8. Standard pad @3.3 V, Voh
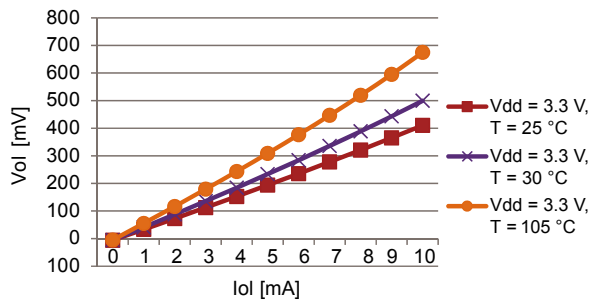
AM040222

Figure 9. Standard pad @3.3 V, Vol
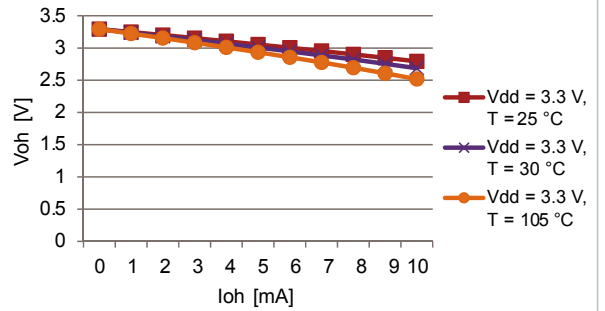
AM040221

Figure 10. Standard pad @5 V, Voh
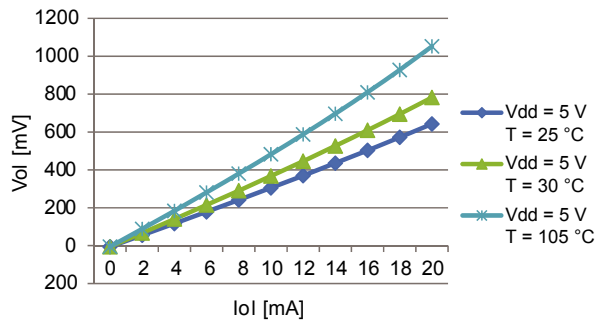
AM040224
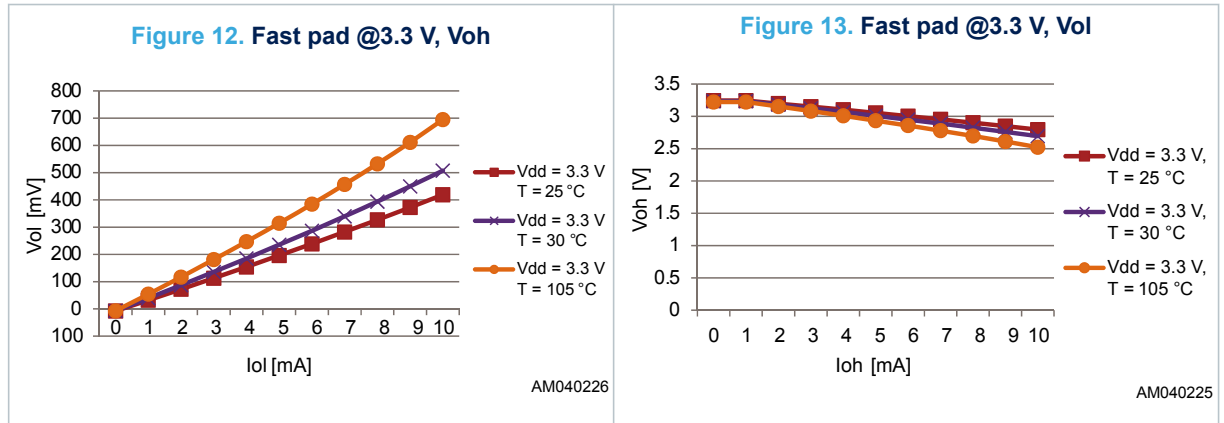
Figure 11. Standard pad @5 V, Vol
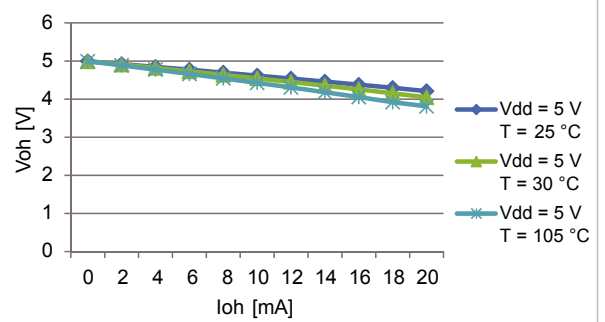
AM040223

5.9.4.2 Fast pad

This pad class is associated to the pins: EFUSE_ENABLE,PWM[0],PWM[1],DT1,DT2

Figure 12. Fast pad @3.3 V, Voh

Figure 13. Fast pad @3.3 V, Vol

Figure 14. Fast pad @5 V, Voh

Figure 15. Fast pad @5 V, Vol
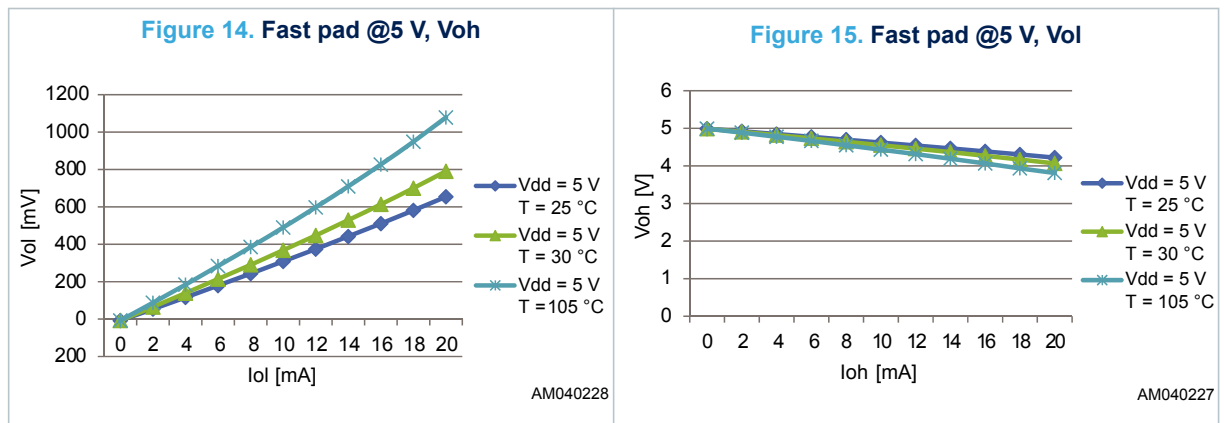
5.9.5 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 14. NRST pin characteristics

Symbol	Parameter	Conditions	Min.[1]	Typ.	Max.[1]	Unit
$V_{IL(NRST)}$	NRST input low level voltage[1]		-0.3		$0.3 \times V_{DD}$	V
$VI_{H(NRST)}$	NRST input high level voltage[1]		$0.7 \times V_{DD}$		$V_{DD} + 0.3$	
$V_{OL(NRST)}$	NRST output low level voltage[1]	I_{OL}= 2 mA			0.5	
$R_{PU(NRST)}$	NRST pull-up resistor[2]		30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse[3]				75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse[3]		500			
$t_{OP(NRST)}$	NRST output filtered pulse[3]		15			µs

1. Data based on characterization results, not tested in production.

2. The RPU pull-up equivalent resistor is based on a resistive transistor.

3. Data guaranteed by design, not tested in production.

5.9.6 I^{2}C interface characteristics

Table 15. I^{2}C interface characteristics

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.[1]	Max.[1]	Min.[1]	Max.[1]	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0[2]		0[2]	900(2)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3.3 to 5 V)[3]		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3.3 to 5 V)[3]		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line[4]		50		50	pF

1. *Data based on standard I^{2}C protocol requirement, not tested in production.*
2. *The maximum hold time of the start condition has only to be met if the interface does not stretch the low time.*
3. *I^{2}C multifunction signals require the high sink pad configuration and the interconnection of 1 kΩ pull-up resistances.*
4. *50 pF is the maximum load capacitance value to meet the I^{2}C std timing specifications.*

5.9.7 10-bit SAR ADC characteristics

The 10-bit SAR ADC parameters are specified under general operating conditions for VDDA and TA unless otherwise specified.

Table 16. ADC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		bit
R_{ADCIN}	ADC input impedance[1]	1			MΩ
V_{IN}	Input conversion voltage range	0		1.25[1][2].	V
$V_{ref\,ADC}$	ADC main reference voltage[3].		1.250		

1. *Maximum input analog voltage cannot exceed V_{DD}/V_{DDA}.*
2. *Exceeding the maximum voltage on VIN, VOUT, ZCD1, ZCD2, VOUT_Efuse,TEMP signals has to be avoided since it may impact the ADC conversion accuracy defined in Table 12*
3. *ADC reference voltage at T_A=25C*

5.9.7.1 ADC accuracy characteristics

See Figure 17 for more details about ADC accuracy parameter definition.

Table 17. ADC accuracy characteristic at V_{DD}/V_{DDA}= 5 V

Symbol	Parameter	Min.[2]	Typ.[1]	Max.[2]	Unit
$|E_O|$	Offset error[3][4]		0.5		
$|E_G|$	Gain error[3][4][5]		0.4		
E_{OG}	Offset + gain error[3][4][5][6]	-8.3		8.9	
E_{OG}	Offset + gain error[1][5][7]	-10.9		10.9	LSB
E_{OG}	Offset + gain error[3][4][5][8]	-13.8		10.9	
$|E_D|$	Differential linearity error[1][2][3]		0.8		
$|E_L|$	Integral linearity error[3][4]		2.0		

1. Operating temperature: TA= 25°C .
2. Data based on characterization results, not tested in production.
3. ADC accuracy vs. negative injection current. The injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended that a Schottky diode (pin to ground) be added to standard analog pins which may potentially inject a negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN}.
4. Results in manufacturing test mode.
5. Gain error evaluated with the two-point method.
6. Temperature operating range: 0°C ≤ T_A ≤ 85°C.
7. Temperature operating range: -25°C ≤ T_A ≤ 105°C.
8. Temperature operating range: -40°C ≤ T_A ≤ 105°C.

5.9.7.2 ADC equivalent input circuit

Figure 16 shows the ADC equivalent input circuit. PLS update block inputs.

Figure 16. ADC equivalent input circuit
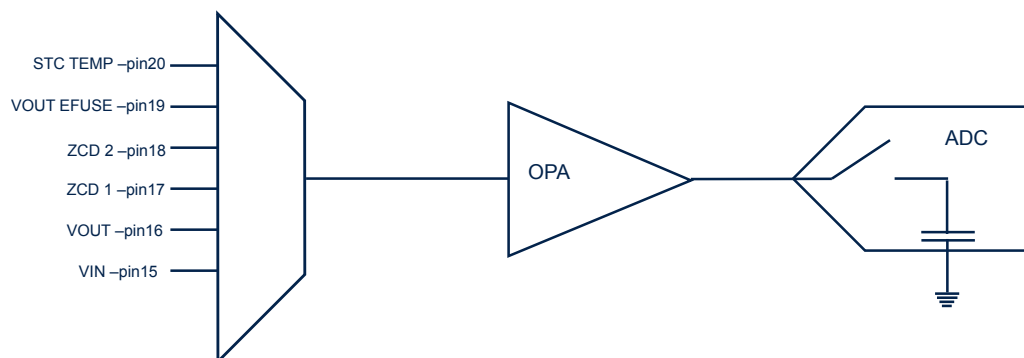
Figure 17. **ADC accuracy parameter definitions**
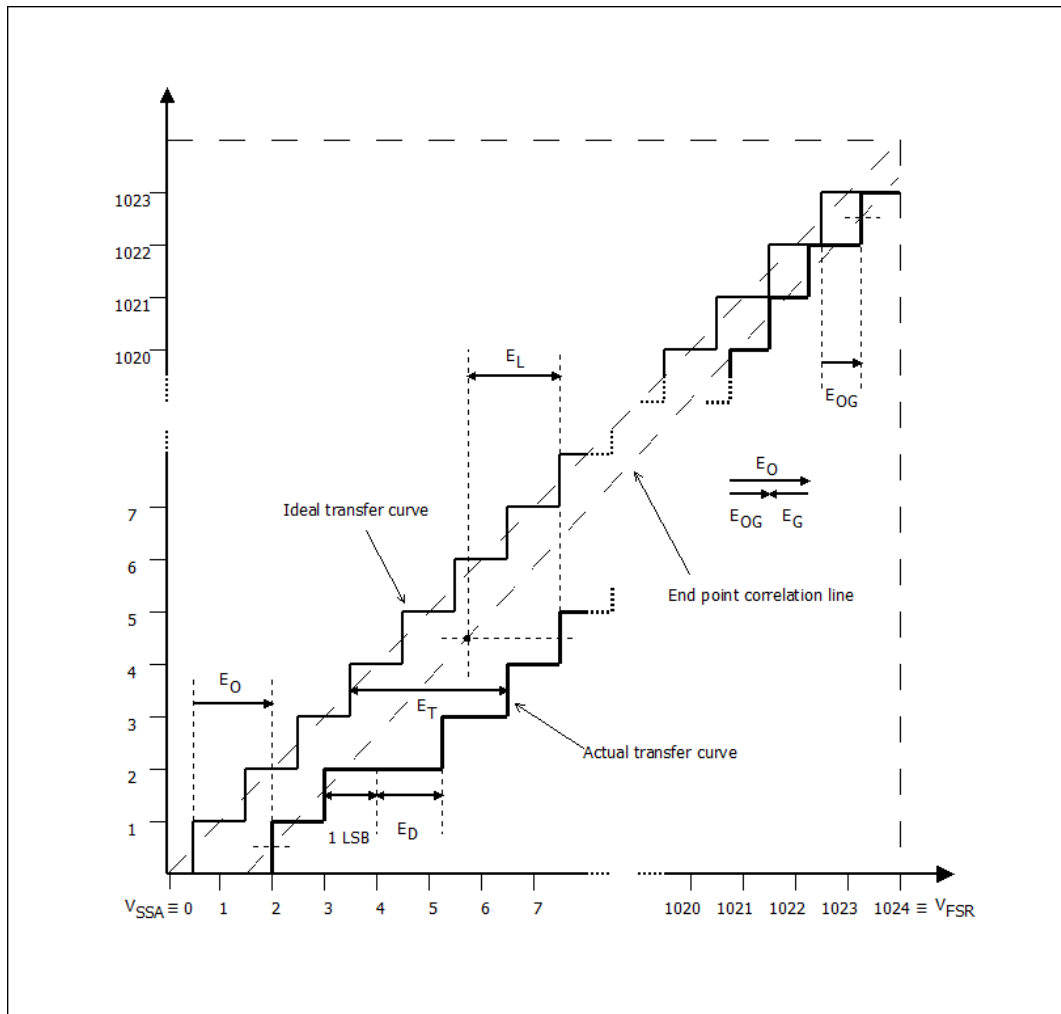
E_T= Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.

E_O= Offset error: Deviation between the first actual transition and the first ideal one.

E_{OG}= Offset+Gain error (1-point Gain): Deviation between the last ideal transition and the last actual one.

E_G= Gain error (2-point Gain): Defined so that E_{OG} = E_O + E_G (parameter correlated to the deviation of the characteristic slope).

E_D= Differential linearity error: Maximum deviation between actual steps and the ideal one.

E_L= Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

6   Thermal characteristics

The STNRG328S functionality cannot be guaranteed when the device is operating under the maximum chip junction temperature(T_{Jmax}).

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W

P_{Dmax} is the sum of $PINT_{max}$ and PI/O_{max} ($P_{Dmax} = PINT_{max} + PI/O_{max}$)

$PINT_{max}$ is the product of IDD and V_{DD}, expressed in Watts. This is the maximum chip internal power.

PI/Omax represents the maximum power dissipation on output pins where: $PI/O_{max} = \Sigma (V_{OL} * I_{OL}) + \Sigma((V_{DD} - V_{OH}) * I_{OH})$, taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level.

Table 18. Thermal characteristics

Symbol	Parameter	Value	Unit
ΘJA	Thermal resistance junction-ambient[1]	26	°C/W

1.   Thermal resistance are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

7 Analog comparators characteristics

Figure 18 shows how the internal comparators are used. Table 19 and Table 20 describe the main comparator paramaters.

Figure 18. Analog Comparators
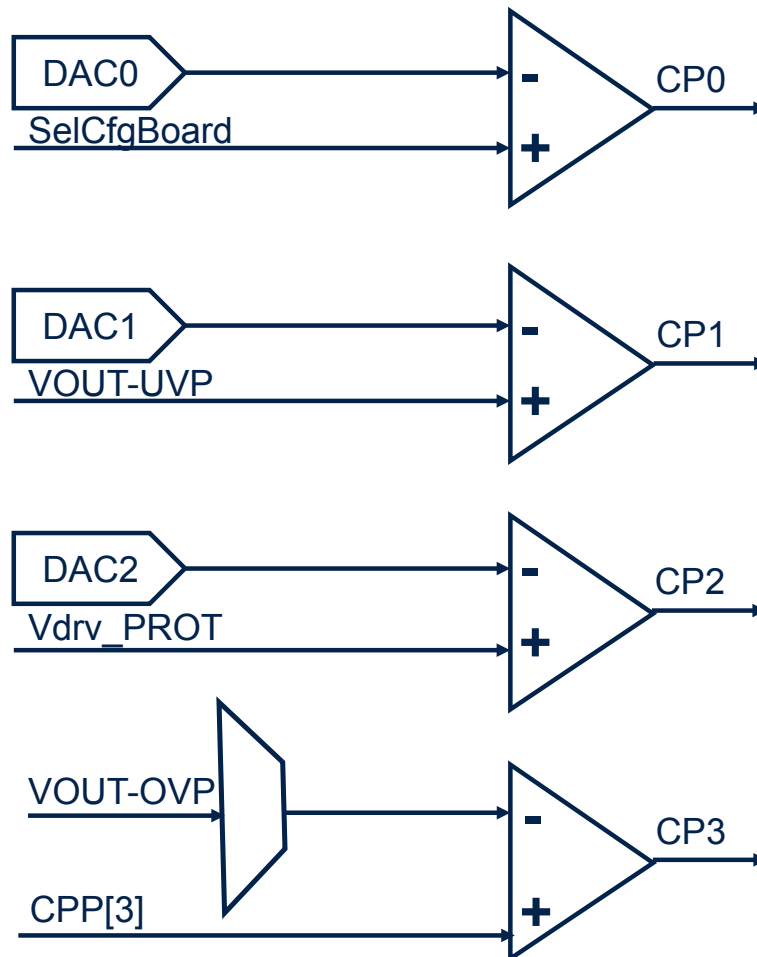
Table 19. Comparator parameters

Symbol	Parameter	Conditions	Min.[1]	Typ.	Max.[1]	Unit
V_{CPP}	Comparator positive input range	-40°C≤ TA≤105°C	0		1.23[2]	V
V_{CPM}	Comparator negative external input voltage range		0		1.23[2] [3]	V
C_{IN}	Input capacitance			3		pF
V_{offset}	Comparator offset error				15	mV
T_{COMP}	Comparison delay time				50[4] [5]	ns

1. *Data based on charcacterization results, not tested in production.*

2. *Maximum analog input voltage cannot exceed V_{DDA}.*

3. *The comparator 3 can be configured with external refernce voltage signal CPM3.*

4. *The overdrive voltage is ± 50 mV.*

5. *This parameter doesn't consider the delay time of comparator signal synchronization stages and SMED logic.*

Table 20. Comparator hysteresis

Symbol	Parameter	Conditions	Hysteresis positive[1]		Hysteresis negative[1]		Unit
			Min.	Max.	Min.	Max.	
V_{HYST0}	Hysteresis voltage code 0	-40°C≤ T_A≤105°C	No hysteresis				mV
V_{HYST1} V_{HYST2}	Hysteresis voltage code 1,2		N.A.				
V_{HYST3}	Hysteresis voltage code 3		4	52	0	-60	
V_{HYST4}	Hysteresis voltage code 4		13	78	-13	-80	
V_{HYST5}	Hysteresis voltage code 5		41	148	-45	150	
V_{HYST6}	Hysteresis voltage code 6		56	203	-58	-205	
V_{HYST7}	Hysteresis voltage code 7		123	406	-125	-403	

1. *Data based on charcacterization results, not tested in production.*

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 Package design overview

Figure 19. **Package drawing VFQFPN32**

BOTTOM VIEW

8.2 Package mechanical data

Table 21. **Package mechanical characteristic VFQFPN32**

Ref.	DATABOOK dimension (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.40	3.45	3.50
E	4.85	5.00	5.15
E2	3.40	3.45	3.50
e		0.50	0.55
L	0.30	0.40	0.50
ddd			0.08

Note:
- *VFQFPN stands for Thermally Enhanced **V**ery thin **F**ine pitch **Q**uad **F**lat **P**ackage **N**o lead.*
- *Very thin profile: 0.80 < A ≤ 1.00 mm.*
- *Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.*
- *Package outline exclusive of any mold flashes dimensions and metal burrs.*

9 Ordering information

Table 22. Ordering information

Part number	Package	Packing
STNRG328S	VFQFPN32	Tube
STNRG328STR	VFQFPN32	Tape and Reel

Revision history

Table 23. Document revision history

Date	Version	Changes
21-Sep-2021	1	Initial release.

Contents

List of tables

List of figures

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