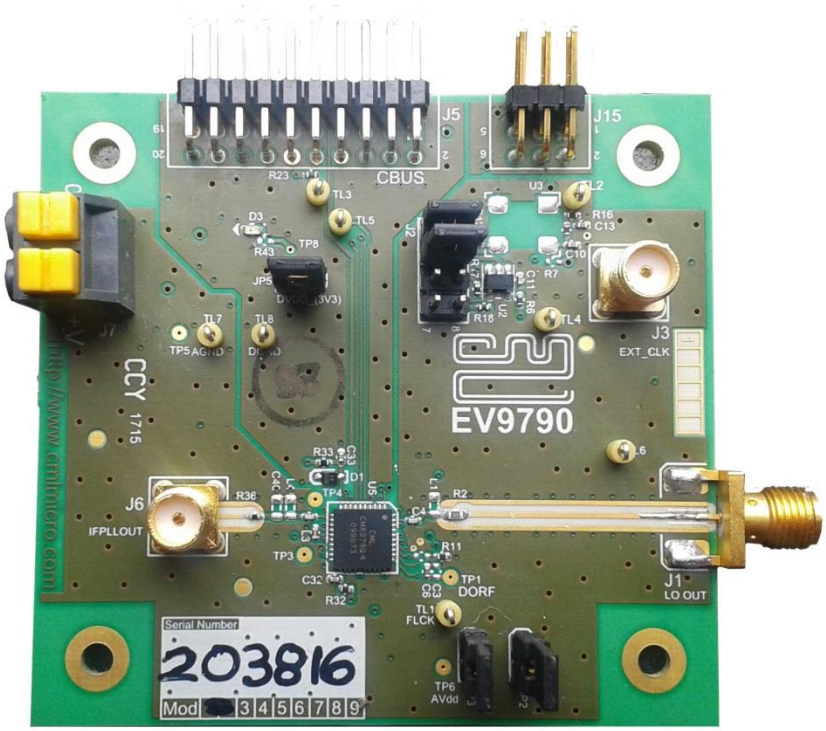
CML Microcircuits
COMMUNICATION SEMICONDUCTORS

# EV9790
# Evaluation Kit for CMX979

UM9790/2 October 2017 **USER MANUAL** Advance Information

## Features

- **Demonstrates the CMX979 Fractional-N RF PLL, IF PLL and associated VCOs**
- **On-board reference oscillator with options for an external source**
- **Divided LO outputs**
- **Powered by external 6.0V power supply**




## 1 Brief Description

The EV9790 is a demonstration and evaluation platform for the CMX979 Dual PLL and VCOs. The CMX979 provides a 2700 to 3600 MHz 24-bit Fractional-N RF PLL with an internal RF VCO. A separate integer-N IF PLL and VCO covering 500 to 1000 MHz (as supplied) are also provided. An inductor value change can configure the IF VCO to cover other frequency ranges. Both VCO outputs can be routed via selectable on- chip frequency dividers.

The board includes all necessary voltage regulators and is operated from an external ~6V dc supply.

The EV9790 provides a 19.2MHz reference oscillator along with options for an additional frequency reference. The EV9790 interfaces to the PE0003 Universal Interface Controller to allow read and write access to the CMX979 registers. A graphical user interface is available for operational set-up as well as handling control scripts.

**CONTENTS**

It is recommended that you check for the latest product datasheet version from the Products page of the CML website: www.cmlmicro.com.

This is Advance Information; changes and additions may be made to this document. Parameters marked TBD or left blank will be included in later issues of this document. Information in this advance document should not be relied upon for final product design.

## 2 History

| Version | Changes | Date |
|---|---|---|
| 2 | References to HB0003 (for engineering samples only) removed as this board no longer needed | 17th October 2017 |
| 1 | First public release - Includes references to HB0003 Interface Board | 12th July 2017 |
| A | Draft | 6th September 2016 |

## 3 Block Diagram

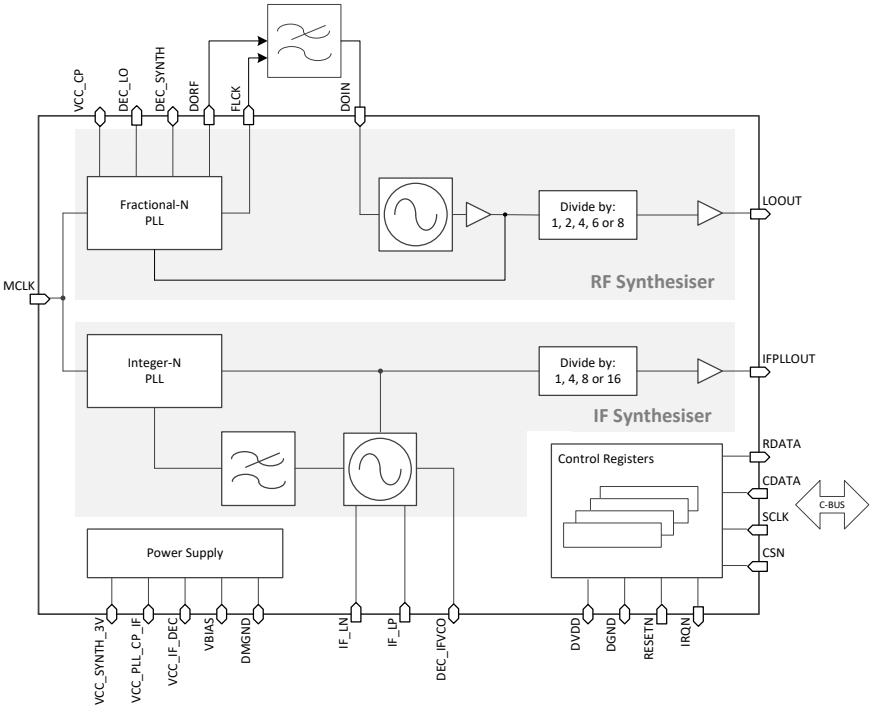



**Figure 1 CMX979 Block Diagram**

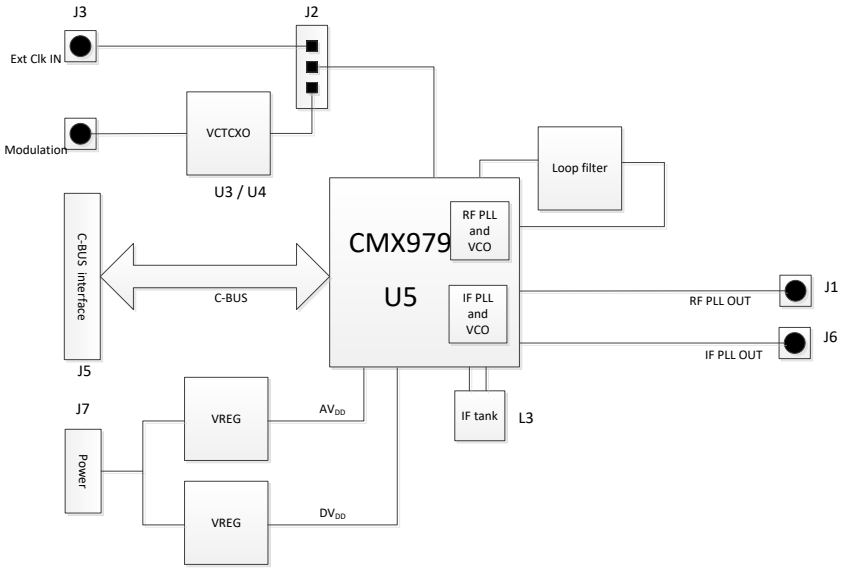



**Figure 2 EV9790 Block Diagram**

# 4 Preliminary Information

The EV9790 provides a complete platform for demonstrating and evaluating the CMX979 (device U5). This document refers to revision B of the EV9790 PCB (PCB596B).

## 4.1 Laboratory Equipment

The following items are essential for evaluation of the EV9790:

- Laboratory power supply
- PE0003 Universal Interface Controller
- PC
- RF spectrum analyser

For more detailed design or investigation work, additional RF test equipment may be required.

### 4.1.1 Power Supply

The input voltage to the PCB at J7 is nominally 6.0V (absolute limits: 5.5V to 8.0V). The 6.0V power supply should be rated at 200mA. On-board regulators provide the 3.3V and 1.8V supplies to the circuits used on the PCB.

NOTE: Care should be exercised with the 6.0V supply as there is the option to power the EV9790 directly from the PE0003 +5V supply via J15, although the additional components for this (L7 and R41) are not fitted as standard. If these components are fitted, an external supply should not be connected to J7. In order to apply an external supply with J15 fitted, L7 and R41 should be removed. Alternatively, the PE0003 could be run from the 6.0V supply.

## 4.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

### 4.2.1 SSD Devices

**This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.**

### 4.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK9790) and notify CML within seven working days if the delivery is incomplete.

## 4.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

## 5 Quick Start

This section provides instructions for users who wish to experiment immediately with this Evaluation Kit. A more complete description of the kit and its uses appears later in this document. The user should also read the appropriate CMX979 datasheet before using the EV9790 board.

NOTES: The default configuration of EV9790 uses the following configuration:

- U4: 19.2MHz frequency reference without buffer.

### 5.1 Setting-Up

The following procedure is recommended:

1. Connect the boards as shown in Figure 3.
2. Ensure that the power supply and reference oscillator selection links are correctly configured.
3. LO Output signals from the RFPLL can be monitored by a spectrum analyser connected to J1.
4. Output from the IF VCO /PLL can be monitored by a spectrum analyser connected to J6 (IF VCO Out).
5. Apply power to the boards.

The boards are now ready for operation.

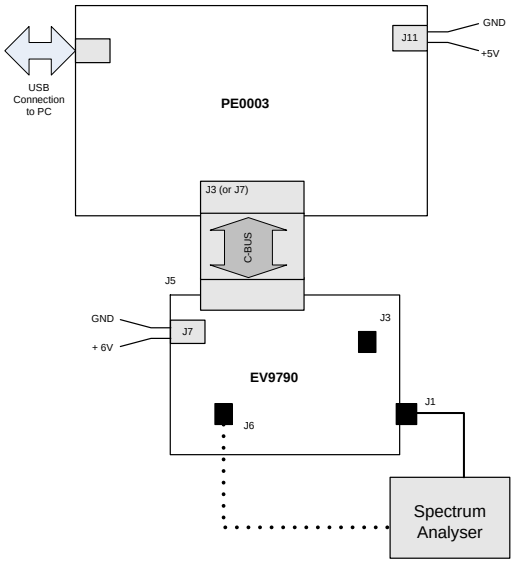



**Figure 3 Typical Evaluation Connections for EV9790**

### 5.2 Operation

When power is applied to the EV9790, the CMX979 will be reset.

### 5.3 Signal Lists

| CONNECTOR PINOUT | | | | |
|---|---|---|---|---|
| **Connector Ref.** | **Connector Pin No.** | **Signal Name** | **Signal Type** | **Description** |
| J1 | N/A | LOOUT | RF | Output from the RF PLL / dividers |
| J3 | N/A | EXT_CLK | RF | External PLL reference clock input |
| J5 | - | - | I/P & O/P | C-BUS control connection |
| J6 | N/A | IFPLLOUT | RF | Output from the IF PLL / dividers |
| J7 | 1 | +V | DC | 6.0V Power supply input |
| J7 | 2 | GNDA | DC | Power supply ground |

**Table 1 Connector List**

| CONNECTOR PINOUT for J5 | | | | |
|---|---|---|---|---|
| **Connector Pin No.** | **Signal Name** | **Signal Type** | **Description** | |
| 1 | RESETN | I/P | Hardware reset | Low to reset, pulled high by R48 |
| 2 | CSN | O/P | Chip Select | |
| 3 | N/C | | No Connection | |
| 4 | CDATA | O/P | Command Data | |
| 5 | N/C | | No Connection | |
| 6 | SCLK | O/P | Serial Clock | |
| 7 | N/C | | No Connection | |
| 8 | RDATA | I/P | Reply Data | |
| 9 | N/C | | No Connection | |
| 10 | IRQN | I/P | Interrupt Request (open-drain) | |
| 11 | GNDD | Power | Connection to Digital Ground | |
| 12 | GNDD | Power | Connection to Digital Ground | |
| 13 to 20 | N/C | | No Connection | |

**Table 2 External C-BUS Host Interface**

| CONNECTOR PINOUT for J15 | | | |
|---|---|---|---|
| **Connector Pin No.** | **Signal Name** | **Signal Type** | **Description** |
| A/1 | DGND_PE0003 | Power | Connection to Digital Ground for PE0003 |
| B/2 | DGND_PE0003 | Power | Connection to Digital Ground for PE0003 |
| C/3 | +5V_PE0003 | Power | Connection to +5V supply from PE0003 |
| D/4 | +5V_PE0003 | Power | Connection to +5V supply from PE0003 |
| E/5 | +5V_PE0003 | Power | Connection to +5V supply from PE0003 |
| F/6 | +5V_PE0003 | Power | Connection to +5V supply from PE0003 |

**Table 3 Optional PE0003 Host /Interface DC connector**

| TEST POINTS | | |
|---|---|---|
| **Test Point Ref.** | **Default Measurement** | **Description** |
| TP1 | - | DORF – RF PLL Charge pump output voltage |
| TP3 | - | VBIAS |
| TP4 | - | VCC_PLL_CP_IF |
| TP5 | - | +V Input supply voltage |
| TP6 | 3.3V | U6 Regulator Output (AVDD) for analogue supplies |
| TP8 | 3.3V | U8 Regulator Output (DVDD) for digital supplies |

**Table 4 Test Points**

| TEST LOOPS | | |
|---|---|---|
| **Test Point Ref.** | **Default Measurement** | **Description** |
| TL1 | | FLCK – Fast Lock output |
| TL2 | | Modulation input for VCTCXO U3 |
| TL3 | | IRQN |
| TL4 | | Modulation input for VCTCXO U4 |
| TL5 | | RDATA |
| TL6 | AGND | Connection to Analogue Ground |
| TL7 | AGND | Connection to Analogue Ground |
| TL8 | DGND | Connection to Digital Ground |

**Table 5 Test Loops**

| JUMPERS | | |
|---|---|---|
| **Ref.** | **Default Setting** | **Description** |
| JP2 | Linked | AVDD – Analogue Supply - Link to enable VCTCXO and buffer supplies |
| JP3 | Linked | AVDD_979 – Link to enable CMX979 analogue supplies |
| JP5 | Linked | DVDD – Link to enable CMX979 digital supplies (C-BUS interface) |
| J2 | Link pin 1 – 2 and pin 3 – 4 | 2 x 4 Pin field for selecting the clock reference source and buffering options<br>To use the on-board VCTCXO, un-buffered, link pins 1-2 & 3-4.<br>To use the on-board VCTCXO, buffered, link pins 2-4 & 7-8.<br>To use an external clock applied to J7, un-buffered, link pins 5-6 & 3-4.<br>To use an external clock applied to J7, buffered, link pins 4-6 & 7-8. |

**Table 6 Jumpers**

Notes:
I/P = Input
O/P = Output
TL = Test Loop
TP = Test Point

## 6 Circuit Schematics and Board Layouts

For clarity, the circuit schematic diagrams are available as separate high-resolution files, which can be downloaded from the CML website. The layout on each side of the PCB is shown in Figure 4 and Figure 5:

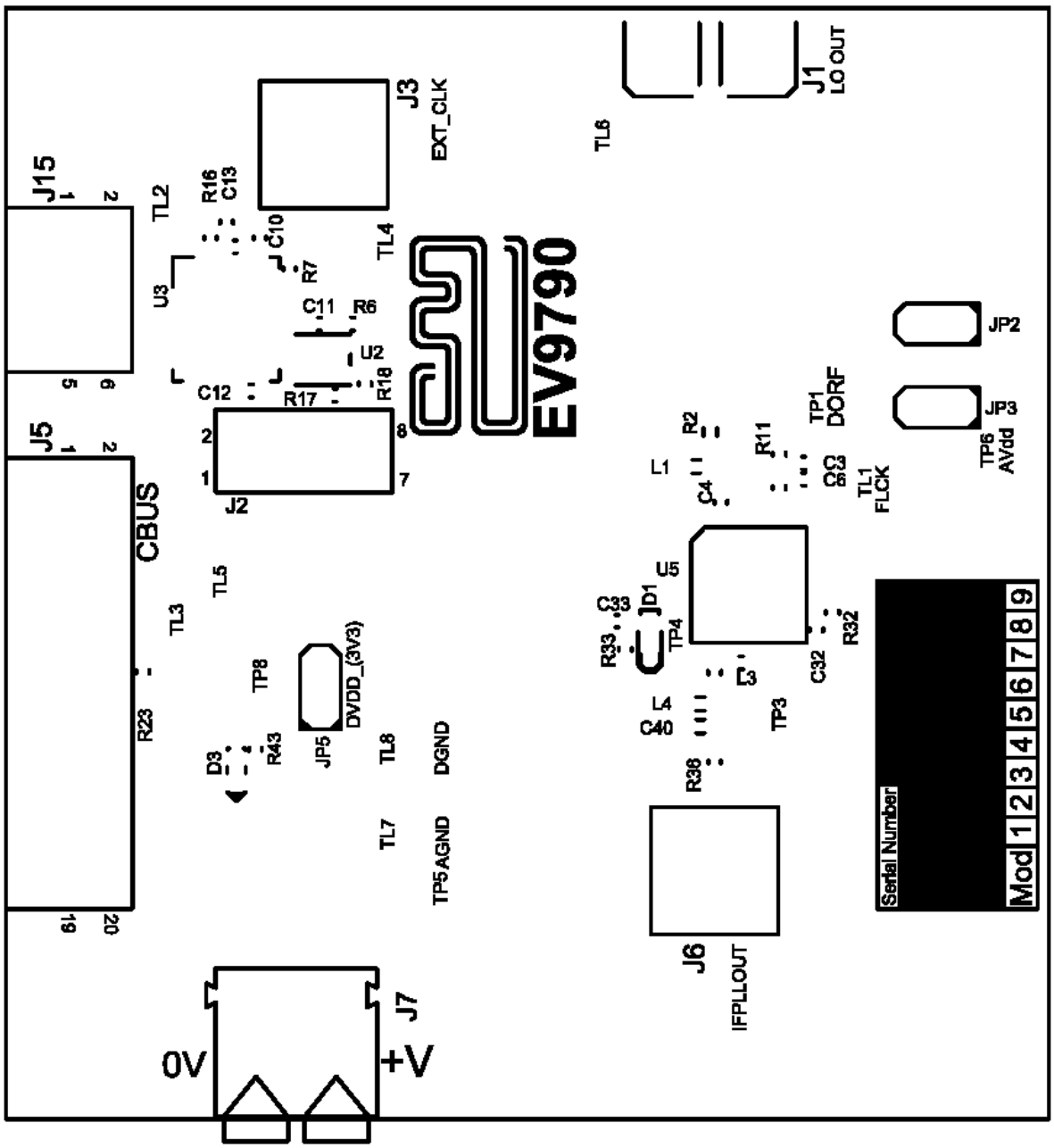



**Figure 4 PCB Layout: Top**

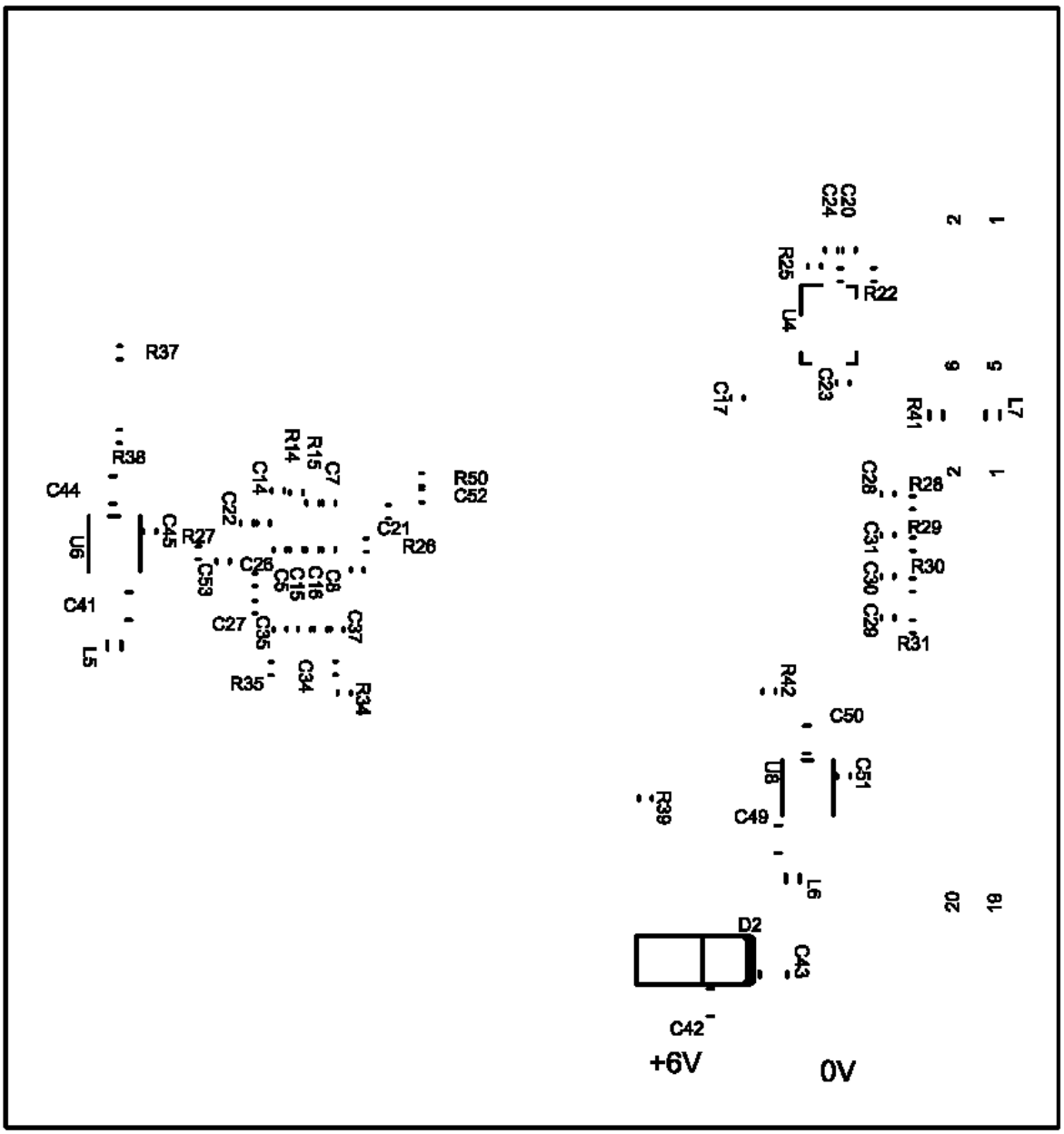



**Figure 5 PCB Layout: Bottom**

# 7 Detailed Description

The EV9790 serves as a demonstrator for the CMX979, a 40-lead VQFN device at location U5.
EV9790 functionality includes:

- 2700 - 3600 MHz VCO and 16- / 24-bit Fractional-N PLL
- IF VCO and Integer-N PLL centred at 900MHz
- 19.2MHz or optional 38.4MHz VCTCXO, plus external reference input
- USB Interface via a PE0003 to a CML standard GUI, to allow script control

## 7.1 Hardware Description

Full details of the silicon functionality are contained in the CMX979 datasheet. The EV9790 is assembled on a 65 x 69mm, 1.6mm thick 6-layer PCB (reference PCB596B), with the upper layer having a Rogers RO4003C ceramic substrate for low loss and consistent high frequency performance. The other layers use FR4 / VT481 2116 dielectric.

In general, RF components, connectors and configuration links have been placed on the top layer, with voltage regulators, supplies and decoupling for the CMX979 on the bottom layer. The layout has been optimised for low ground impedance and short RF tracking for operation at high frequencies. Gerber files and a BOM can be downloaded from the CML website.

A high frequency SMA edge connector is used for the J1 output with a Grounded Co-Planar Wave Guide transmission line.

### 7.1.1 RF VCO /PLL

The CMX979 contains a 16- or 24-bit Fractional-N PLL synthesiser used with the on-chip 2700 – 3600 MHz VCO. The loop filter is external to the IC and can (optionally) incorporate a fast locking function, see Figure 6. The loop filter output is then routed back to the tuning input of the internal VCO,. The on-chip VCO output is available off-chip either as a fundamental or divided by 2, 4, 6 or 8 at J1.

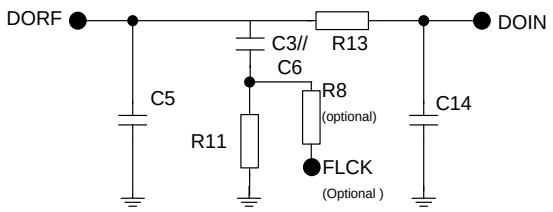



**Figure 6 Example External Components – VCO External Loop Filter**

| VCO Frequency | C5 | C3//C6 | C14 | R11 | R13 | R8 (optional FLCK) |
|---|---|---|---|---|---|---|
| 2.925GHz | 750pF | 6.2nF | 27pF | 1.6kΩ | 5.1kΩ | See Datasheet section 7.3.4 |
| 3.5GHz | 470pF | 3.6nF | 22pF | 2.4kΩ | 6.8kΩ | See Datasheet section 7.3.4 |
| Values Fitted | 680pF | 5.6nF | 27pF | 2.2kΩ | 5.6kΩ | See Datasheet section 7.3.4 |

Note: C3, C5, C14, R11 and R13 assume a Kvco=70MHz/V, Icp=400uA, Fref=19.2MHz. The values fitted are a compromise for mid-band operation. These values may require modification for use with other comparison frequencies and charge pump currents.

**Table 7 3rd Order Loop Filter Values for a VCO Frequency of 2.925GHz/3.5GHz**

### 7.1.2 IF PLL/VCO

The CMX979 incorporates an additional internal IF VCO and PLL with internal loop filter. The VCO is tuned by external inductor L3; with the default value fitted the tuning range is centred around 900MHz. The VCO output is available either as a fundamental or divided by 4, 8 or 16 at the SMA connector J6.

### 7.1.3 Reference Oscillator

U4 is a GTXO-91T/EI 19.2MHz 0.5 ppm TCXO, part number MP05955, supplied by Golledge (www.golledge.com). This is used as the reference for the RF and IF PLLs within the CMX979 (MCLK). Options are provided to use a lower phase noise Golledge GTXO-74V/JI 38.4MHz VCTCXO reference, part number MP07489 (footprint U3) or an external reference signal can be applied to the SMA connector J3. These inputs can also be buffered via U2. The selection of this buffering is via the link configuration field J2. The VCTCXO tuning inputs can be accessed via test loops TL2 and TL4, to allow the addition of a modulating signal within the PLL bandwidth. Note that if the alternative oscillator footprint U3 is used, both the supply resistor R22 and output coupling capacitor C23 should be removed to disable the unused oscillator U4.

#### 7.1.4 Power Supplies

The input to the PCB is nominally 6.0V (absolute limits: 5.5V to 8V) applied to J7. Reverse polarity protection is provided by D2. On-board regulators (U6, U8) are provided to generate the 3.3V and 1.8V supplies used on the EV9790. A green LED on the digital supply (D3) confirms that power is correctly applied.

#### 7.1.5 Reset Circuit

An RC circuit is provided (R33, C33) to hold the RESETN pin low momentarily at power-up. Diode D1 is to discharge the capacitor quickly when powering down the board.

#### 7.1.6 Inductors

All inductors used in the RF sections of the design are manufactured by Coilcraft (www.coilcraft.com). Performance of the circuits with inductors from other manufacturers may vary.

## 7.2 Adjustments and Controls

The only user hardware control on the board is the ability to select input buffering of the reference oscillator U4 or an external source. This is described in section 7.1.3. All other control is via C-BUS and the GUI described in the next section.

## 7.3 Script/GUI Control

To investigate the performance and features of the EV9790 in more detail, a Windows GUI can be used to control the CMX979 via a PE0003 controller – either by manual register accesses or by running scripts. The GUI is common to the EV9750 Evaluation Kit, so is referred to as ES9750, and can be found in 'ES9750xx.zip'.

Setting-Up

- Copy the file 'ES9750xx.zip', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect a dc supply to the PE0003 Universal Interface Card and set supply voltage level to 5V / 500mA current limit.
- Connect a dc supply to the EV9790 and set the voltage level to 6V / 250mA current limit.
- Attach a USB cable between the PE0003 Universal Interface Card and the USB port of the PC.
- Turn on the power supplies.

Install the USB driver when requested. The driver is in the same folder as the 'ES9750xx.zip' files were extracted to (..\Driver). Follow instructions on the screen to install the USB driver. Select the 'Install this driver software anyway' option when the Message Box below is displayed:

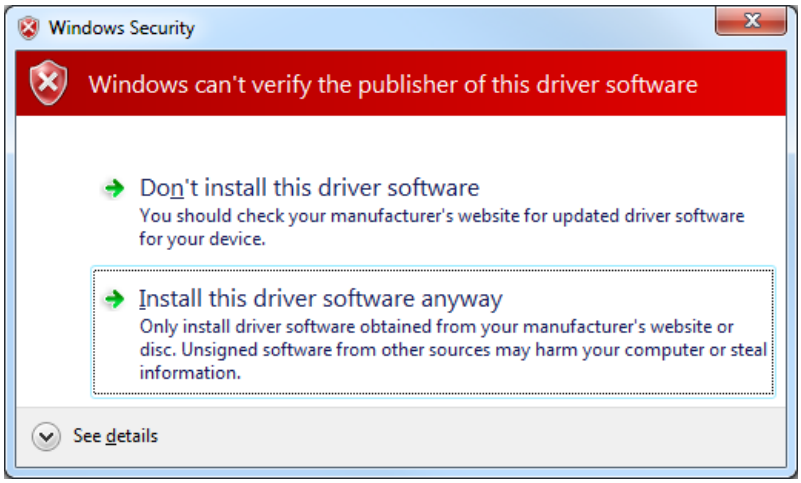



**Figure 7 Driver Verification Dialogue**

The executable ES9750xx.EXE can now be run. This software is for the family of CMX975 – CMX979 devices. Select the radio button for the CMX979 IC.

There are six sheets within the tabbed dialog box structure. These are described in the following sections.

### 7.3.1 The C-BUS Control Tab

This tab provides basic C-BUS read, write and general reset functions. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The radio buttons select an 8-bit or 16-bit read/write operation. The lengths of the entered values are limited to 2 characters (1 byte) for read or write register addresses and 2 or 4 characters (1 or 2 bytes) for the register write data. The General Reset button writes 00H to the CMX979 device.

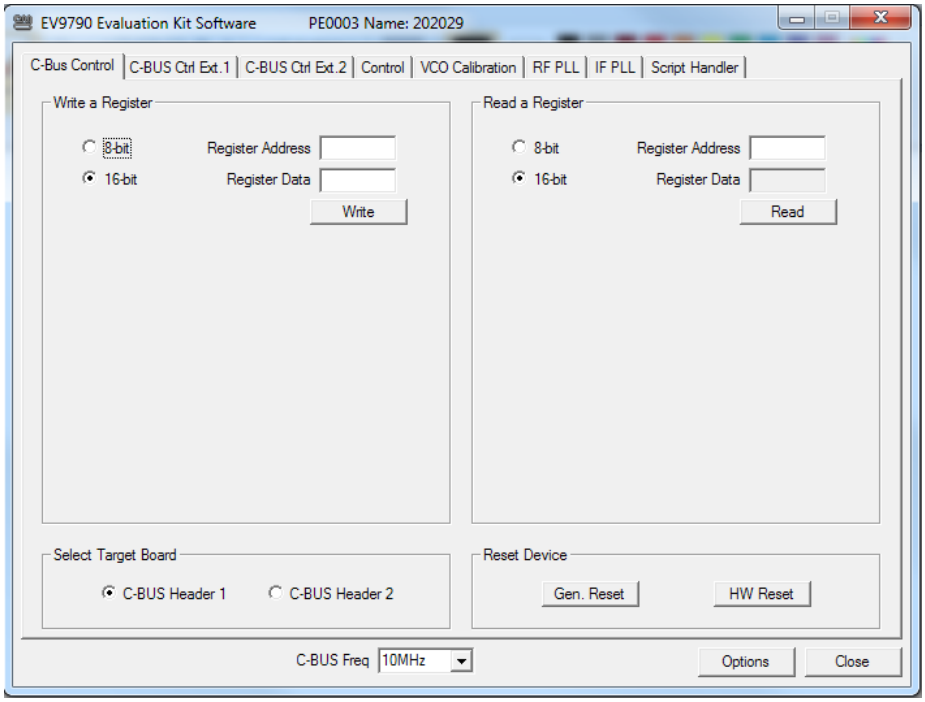



**Figure 8 C-BUS Control Tab**

### 7.3.2 The C-BUS Control Extended Tabs (C-BUS Ctrl Ext. 1 / Ext. 2)

These tabs provide multiple C-BUS read and write functions. Each row in the table represents a single action on a C-BUS register. Select the C-BUS register type from the drop down list. The Update button and the Data edit box will be configured according to the selection. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The lengths of the entered values are limited to 2 characters (1 byte) for register addresses and 2 or 4 characters (1 or 2 bytes) for the register data. Click the Update button to read or write a single C-BUS register. For multiple C-BUS read or write operations, select the C-BUS registers using the Enable check boxes and click on the 'Wr all', 'Rd all' or 'Wr\Rd all' buttons. Click on the 'Wr all' button to write all the selected write type C-BUS registers. Click on the 'Rd all' button to read all the selected read type C-BUS registers. Click on the 'Wr\Rd all' button to read or write all of the selected C-BUS registers. Two separate tabs are used as one may be used to control a device on the other PE0003 C-BUS port.

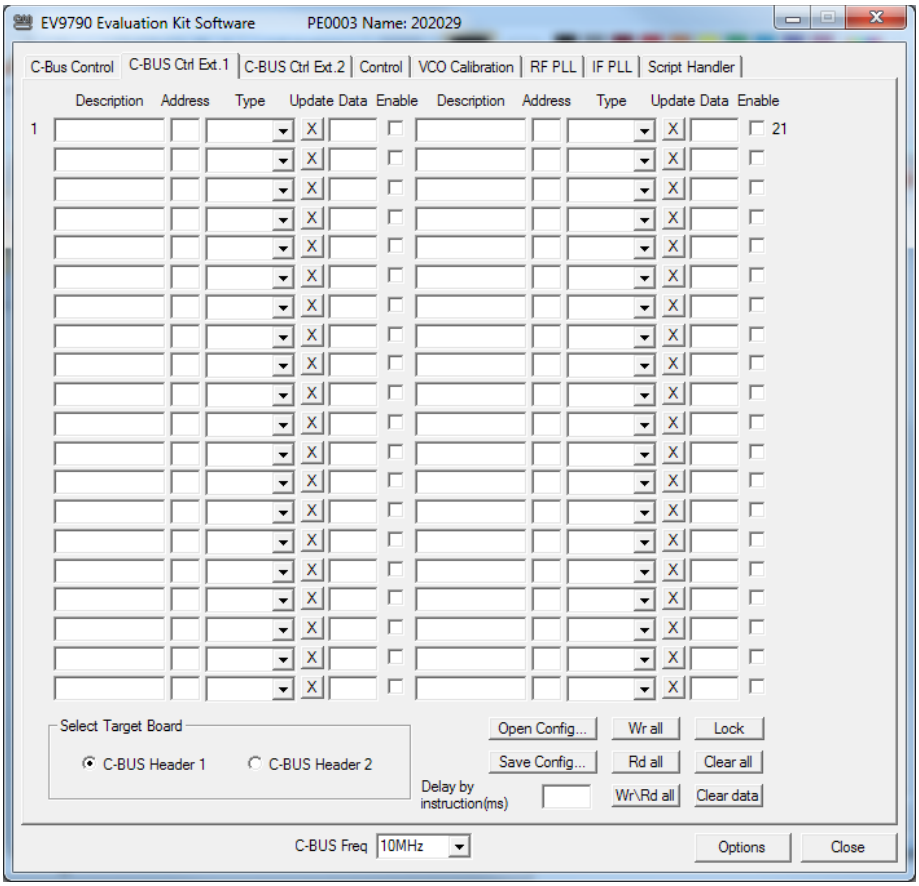



**Figure 9 C-BUS Control Extended Tab**

The C-BUS actions in the table are executed sequentially, starting at "1" (top left of the table). The 'Delay by instruction (ms)' box introduces a delay between the execution of each C-BUS action (default = no delay).

Click on the 'Clear all' button to reset the table. Click on the 'Clear data' button to reset the Data edit boxes.

The 'Lock' button may be used to disable the Description, Address and Type controls, preventing accidental changes. Click on the 'Lock' button again to re-enable these controls.

Use the 'Save Config…' button to save the current table. The Description, Address, Type, Data and Select columns are saved in the specified file. Use the 'Open Config…' button to load a previously saved table.

### 7.3.3 The General Control Tab

This tab provides access to registers for general control of the device functions, e.g. to write to the General Control register and read back from the Device Status register. This tab can also provide control of the RF LO output divider.

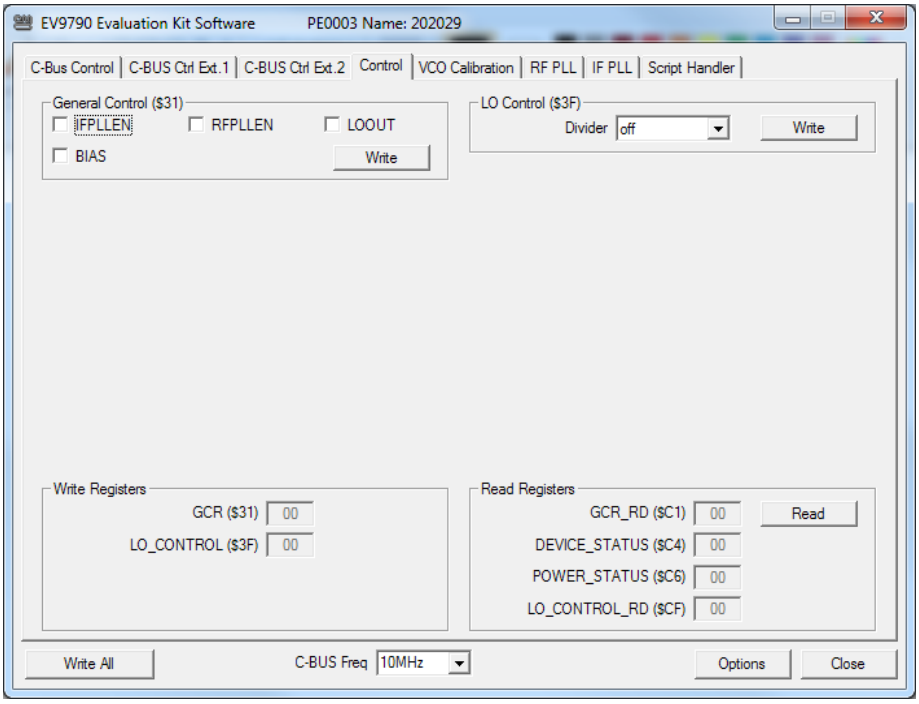



**Figure 10 General Control Tab**

### 7.3.4 The VCO Calibration Tab

This tab provides access to the RF and IF VCO calibration controls. Tick boxes are available to provide automatic calibration, or alternatively, fixed values can be written to the appropriate registers. The returned calibration values can be read back, along with an indication of the calibration status flags.

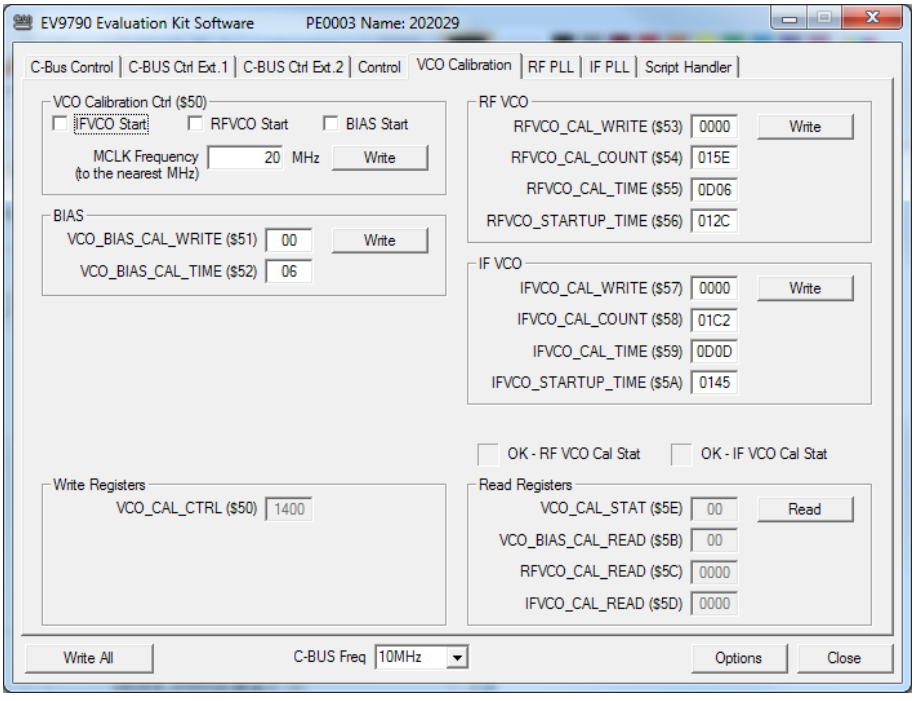



**Figure 11 VCO Calibration Tab**

### 7.3.5 The RF PLL Tab

This tab provides access to the RF PLL functions including charge pump current, fast lock functions and lock detection. This includes a calculator to determine the register values for a given reference (MCLK), comparison and wanted VCO output frequency.

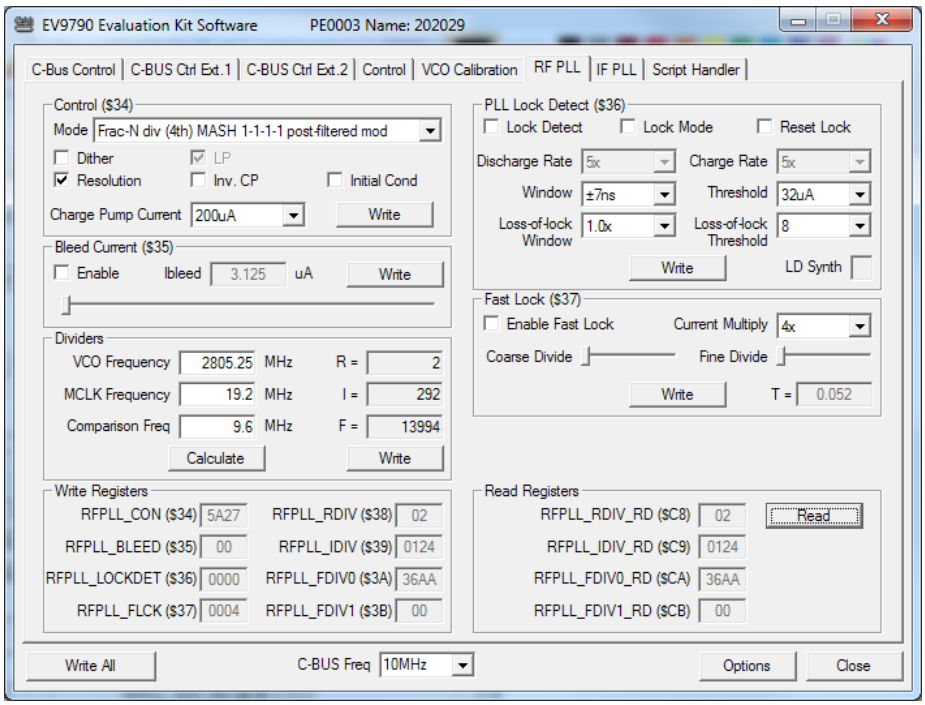



**Figure 12 RF PLL Tab**

### 7.3.6 The IF PLL Tab

This tab provides access to the IF PLL functions. This includes a calculator to determine the register values for a reference (MCLK), comparison and wanted VCO output frequency. There are also drop-down selections for the IF and RF output dividers.

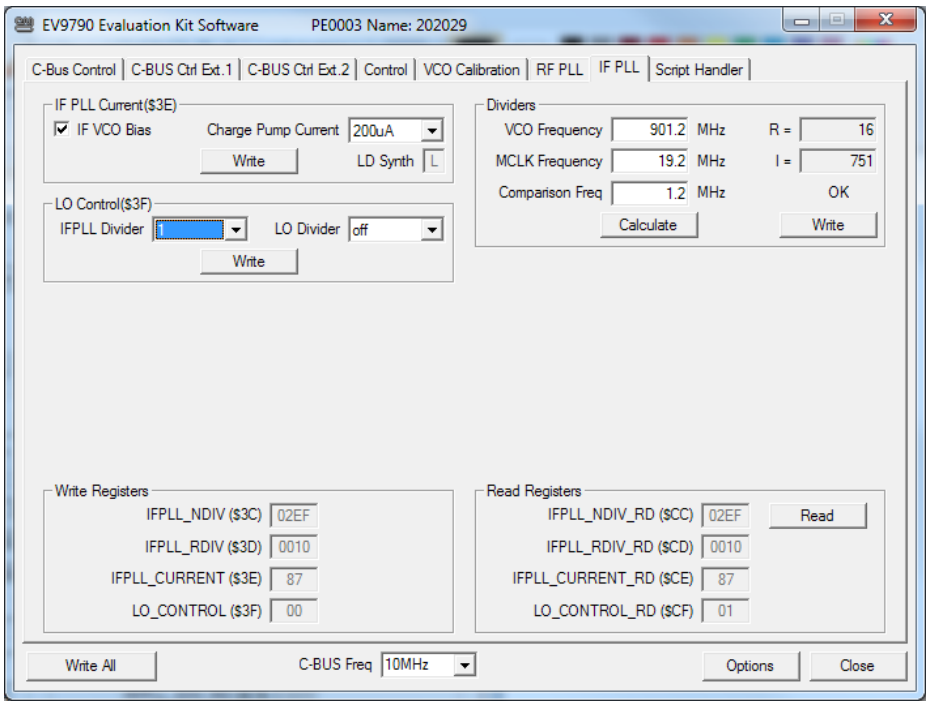



**Figure 13 IF PLL Tab**

### 7.3.7 The Script Handler Tab

The Script Handler tab allows the execution of scripts. These are plain text files on the host PC which are compiled by the GUI, but executed on the ARM Microprocessor on the PE0003. The script language is documented separately in the "Script Language Reference" document, which can be downloaded with the PE0003 support package from the CML website at www.cmlmicro.com. The following are two demonstration scripts developed for the EV9790 Evaluation Kit:

**EV9790_RFPLL 3G2 19M2.pes**

This script locks the RF VCO / PLL at 3.2GHz using the '1100' 16-bit Fractional-N mode with the output at 1.6GHz (divide by 2 output enabled). A 19.2MHz comparison frequency is used with 400µA charge pump current. Both RF VCO and bias calibrations are performed and the results displayed. For additional confidence, the PLL divider registers are also read back.

**EV9790_IFPLL.pes**

This script locks the IF VCO / PLL at 901.2MHz. A 1.2MHz comparison frequency is used with 400uA charge pump current. Both IF VCO and bias calibrations are performed and the results displayed. For additional confidence, the PLL divider registers are also read back.

To select a script file, click on the 'Select Script' button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the '>' button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the 'Save Results' or 'Clear Results' buttons, respectively. When a script file is being executed, the 'Run Script' button will change to be the 'Abort' button, the rest of the tab will be disabled and the other tabs cannot be selected.

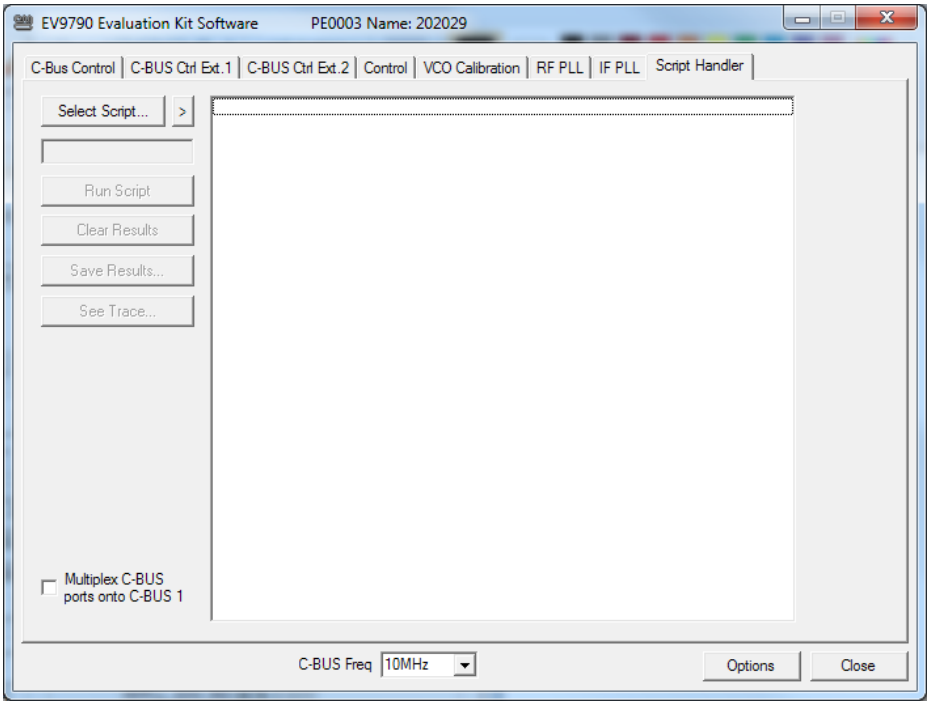
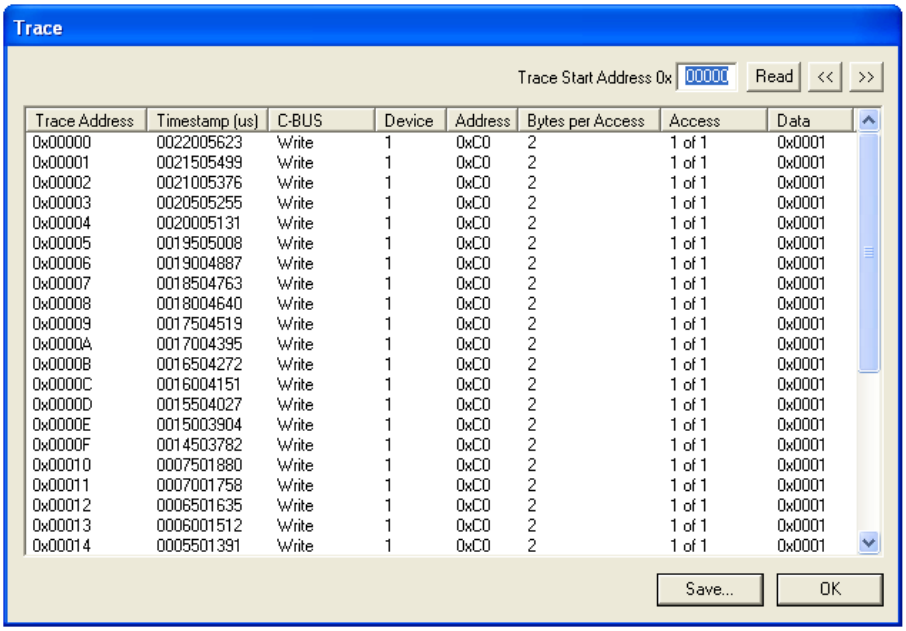



**Figure 14 Script Handler Tab**

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Click on the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.




| Trace Address | Timestamp (us) | C-BUS | Device | Address | Bytes per Access | Access | Data |
|---|---|---|---|---|---|---|---|
| 0x00000 | 0022005623 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00001 | 0021505499 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00002 | 0021005376 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00003 | 0020505255 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00004 | 0020005131 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00005 | 0019505008 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00006 | 0019004887 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00007 | 0018504763 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00008 | 0018004640 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00009 | 0017504519 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000A | 0017004395 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000B | 0016504272 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000C | 0016004151 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000D | 0015504027 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000E | 0015003904 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x0000F | 0014503782 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00010 | 0007501880 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00011 | 0007001758 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00012 | 0006501635 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00013 | 0006001512 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |
| 0x00014 | 0005501391 | Write | 1 | 0xC0 | 2 | 1 of 1 | 0x0001 |

**Figure 15 Trace Dialog Box**

Click on the '>>' or '<<' buttons to upload and display the next or previous C-BUS transaction data block. Click on the 'Read' button to upload and display the C-BUS transaction data block starting at the address displayed in the Trace Start Address edit box. Use the 'Save…' button to save the trace data to a file.

## 7.4 Application Information

See Section 5.1 for board setup details and Section 5.2 for operation of the EV9790.

### 7.4.1 Typical Performance

Typical performance for the EV9790 is shown below.

The phase noise profiles can be varied by a number of settings, notably the loop filter bandwidth, comparison frequency, charge pump current, reference noise, output divider setting, etc.

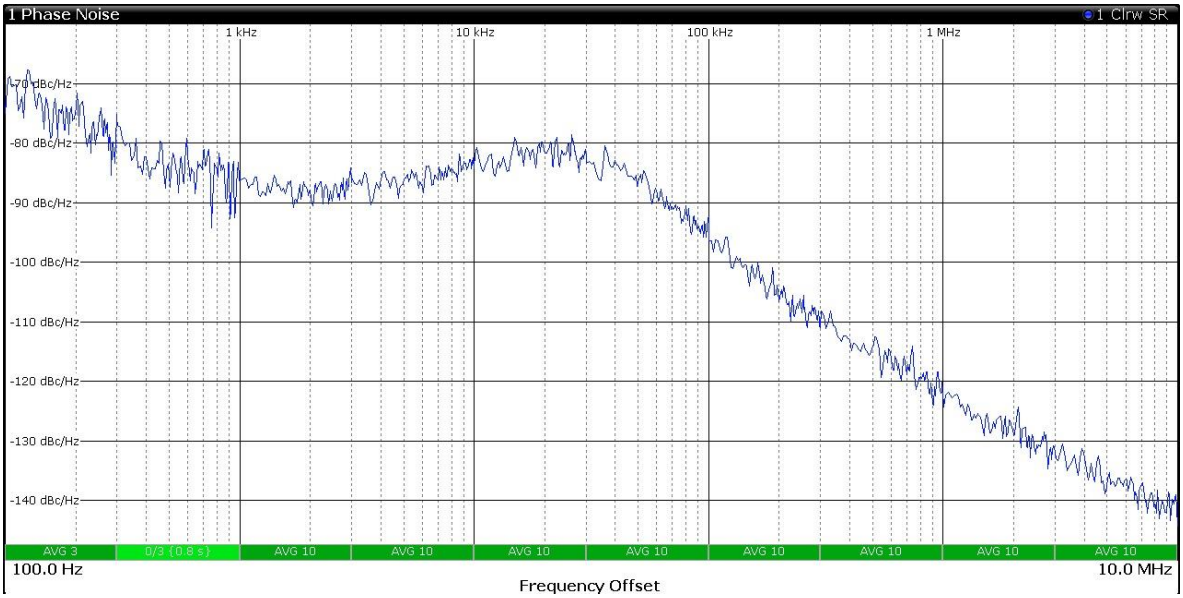



**Figure 16 Phase noise plot of 2.8GHz RF PLL, Icp=400µA, $F_{Comp}$ =19.2MHz, PLL type '1100'.**

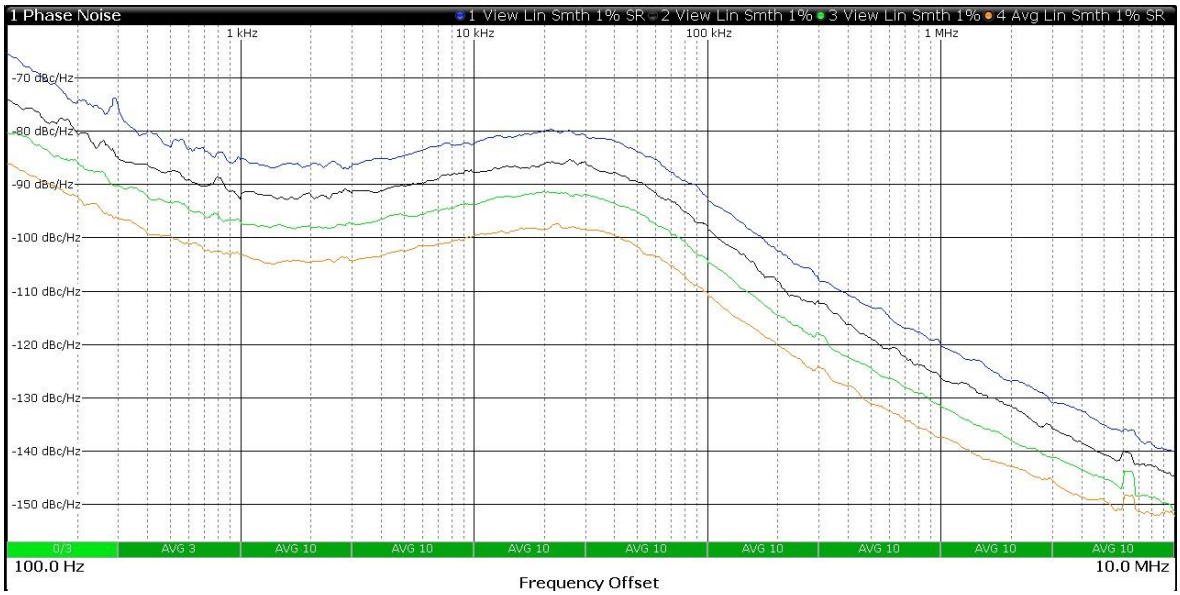



**Figure 17 Phase noise plot of 3.2GHz RF PLL, Icp=400µA, $F_{Comp}$ =19.2MHz, PLL type '1100' also showing output in /2 mode (1600MHz), /4 mode (800MHz) and /8 mode (400MHz).**

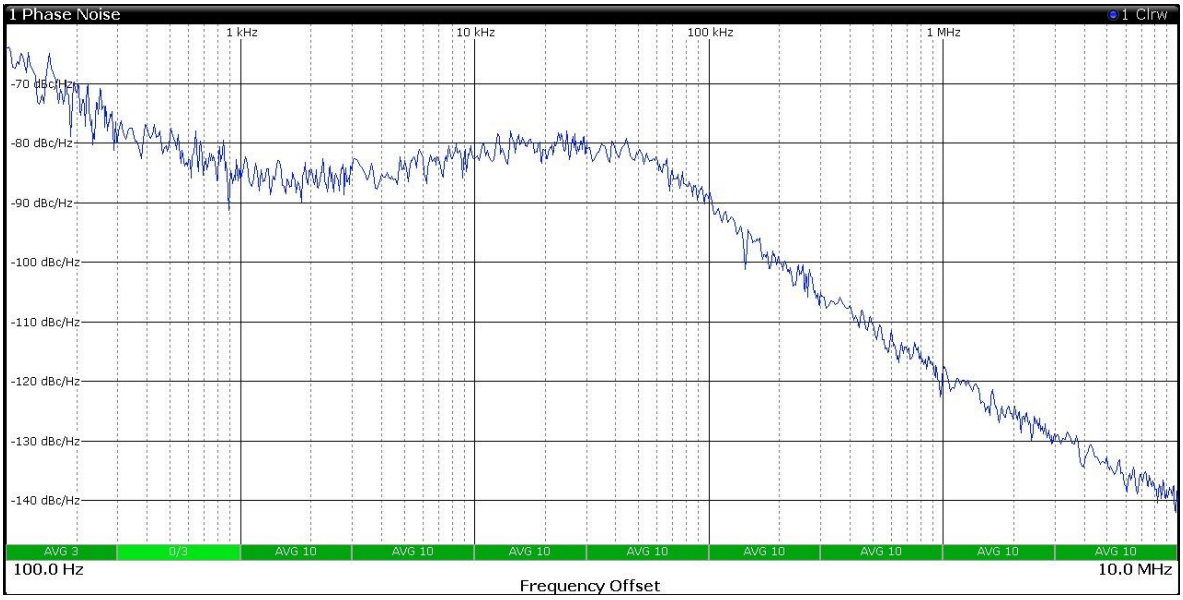



**Figure 18 Phase noise plot of 3.6GHz RF PLL, Icp=400µA, $F_{Comp}$ =19.2MHz, PLL type '1100'.**

The IF PLL has a typical phase noise profile as shown in the plots below, using the default L3 inductor value. The effect of the divider is demonstrated in Figure 20.

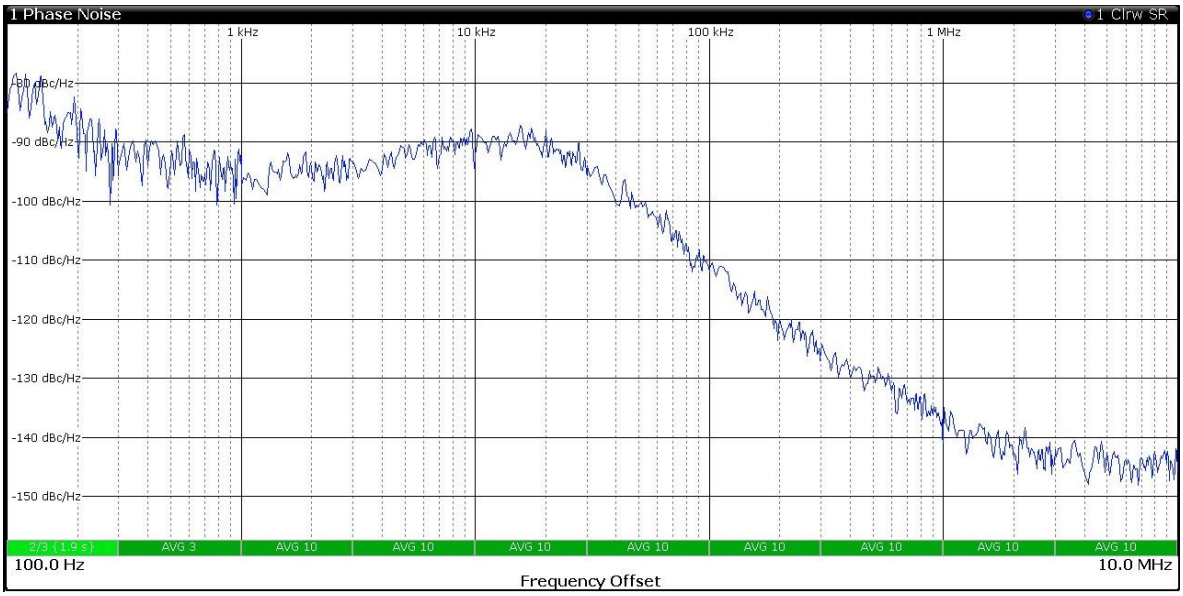



**Figure 19 Phase noise plot of 900MHz IF PLL, Icp= 400µA, $F_{Comp}$ =1.2MHz**

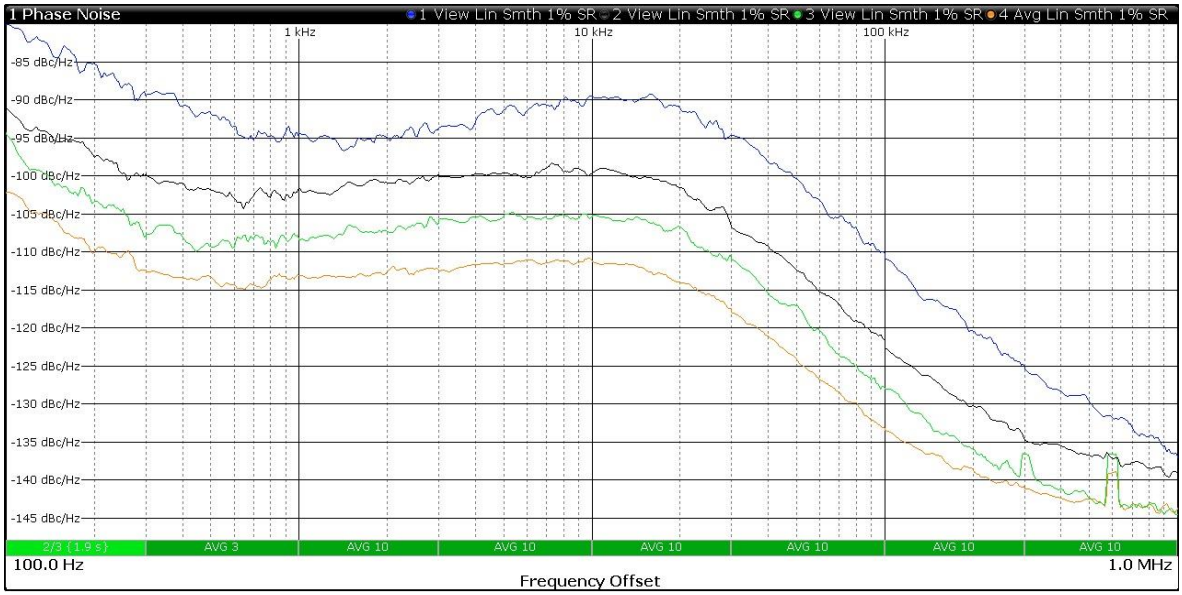



**Figure 20 Phase noise plot of 900MHz IF PLL, Icp= 400µA, $F_{Comp}$ =1.2MHz, also showing the effects of selecting the /4 (225MHz), /8 (112.5MHz) and /16 (56.25MHz) outputs.**

## 7.5 Troubleshooting

The EV9790 is a complex RF system. If incorrectly programmed or modified, results will be at variance from datasheet performance. Please study the CMX979 datasheet, along with the User Manuals, associated schematics and layout drawings for the EV9790 board when troubleshooting. This section provides suggestions to help users resolve application issues that may be encountered.

### 7.5.1 RF PLL Operation

| Error Observed | Possible Cause | Remedy |
|---|---|---|
| PLL output unstable / noisy but on frequency | Unstable / low reference input level | Check the input reference connections and level. Check operation using the default on-board reference. |
| | Loop instability | The programmed PLL values may give a high gain peak. Check the loop components fitted and reprogram with a higher charge pump current or comparison frequency. |
| VCO not close to programmed frequency | Not calibrated. | Run auto calibration of the RFVCO and bias using the VCO calibration tab. |
| | | Check continuity of the loop filter. |
| | Incorrect programming | Check that the correct output division ratio has been selected |

**Table 8 RF PLL – Possible Errors**

### 7.5.2 IF PLL Operation

| Error Observed | Possible Cause | Remedy |
|---|---|---|
| PLL output unstable / noisy but on frequency | Loop instability | The programmed PLL values may give a high gain peak. Check the pump current or comparison frequency selected. |
| VCO not close to programmed frequency | Not calibrated. | Run auto calibration of the IFVCO and bias using the VCO calibration tab. |
| | Incorrect programming | Check that the correct output division ratio has been selected |

**Table 9 IF PLL – Possible Errors**

# 8 Performance Specification

## 8.1 Electrical Performance

### 8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

| | Min. | Max. | Units |
|---|---|---|---|
| Supply ($V_{IN}$ - $V_{SS}$) | 0 | 8.0 | V |
| Current into or out of $V_{IN}$ and $V_{SS}$ pins | 0 | +0.5 | A |
| Current into or out of any other connector pin | -20 | +20 | mA |
| Maximum Input Level | | +10 | dBm |

### 8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

| | Notes | Min. | Max. | Units |
|---|---|---|---|---|
| Supply ($V_{IN}$ - $V_{SS}$) | | 5.5 | 8.0 | V |

### 8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 19.2MHz, $V_{IN}$ = 6.0V, $T_{AMB}$ = +25°C.

| | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **DC Parameters** | | | | | |
| $I_{IN}$ (Regulators and reference on, CMX979 in reset) | 1 | – | 6.5 | – | mA |
| $I_{IN}$ (CMX979 RF PLL and VCO enabled, LO OUT enabled, divide by 1 ) | 1 | – | 45 | – | mA |
| $I_{IN}$ (IF PLL enabled, divide by 1 output) | 1 | – | 16 | – | mA |
| $I_{IN}$ (CMX979 IF and RF PLLs and VCOs enabled) | 1 | – | 52 | – | mA |
| **RF PLL / VCO Parameters** | | | | | |
| Frequency Range | | 2700 | – | 3600 | MHz |
| Divide by 2 Output Range | | 1350 | | 1800 | MHz |
| Divide by 4 Output Range | | 675 | | 900 | MHz |
| Divide by 6 Output Range | | 450 | | 600 | MHz |
| Divide by 8 Output Range | | 337.5 | | 450 | MHz |
| RF output, J1 | 2,3 | – | -7 | – | dBm |
| Output Impedance | | – | 50 | – | Ω |
| Phase Noise (typical) at MHz, 10kHz offset | | – | TBD | – | dBc/Hz |
| **IF PLL / VCO Parameters** | | | | | |
| Frequency Range | 4 | 700 | 900 | 1000 | MHz |
| Divide by 4 Output Range | | 175 | | 250 | MHz |
| Divide by 8 Output Range | | 87.5 | | 125 | MHz |
| Divide by 16 Output Range | | 43.75 | | 62.5 | MHz |
| RF output, J6 | 2,3 | – | -10 | – | dBm |
| Output Impedance | | – | High8k // 0.6pF | – | Ω |
| **Reference input (Ext Clk)** | | | | | |
| Input Impedance | | – | High | – | Ω |
| Sensitivity | 5 | – | -20 | – | dBm |
| **Microcontroller Interface** For timings see CMX979 Datasheet | | | | | |

**Notes:**

1. PCB current consumption, not current consumption of the CML devices.
2. Unmatched
3. 
4. Using the default value of inductor L3 (8.2nH).
5. Measured at J3 from a 50 Ω source.
6. 

This is Advance Information; changes and additions may be made to this document. Parameters marked TBD or left blank will be included in later issues of this document. Information in this advance document should not be relied upon for final product design.

CML Microcircuits
COMMUNICATION SEMICONDUCTORS

| | | |
|---|---|---|
| United Kingdom | tel: +44 (0) 1621 875500 | email: sales@cmlmicro.com<br>techsupport@cmlmicro.com |
| Singapore | tel: +65 62888129 | email: sg.sales@cmlmicro.com<br>sg.techsupport@cmlmicro.com |
| United States | tel: +1 336 744 5050<br>800 638 5577 | email: us.sales@cmlmicro.com<br>us.techsupport@cmlmicro.com |

www.cmlmicro.com