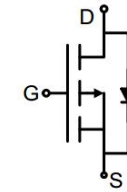
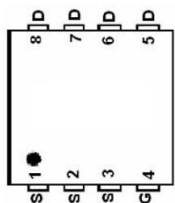
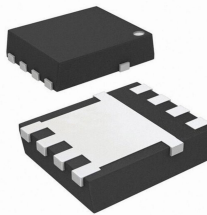


P-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The GT700P08D3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} -80V ● I_D (at $V_{GS} = -10V$) -16A ● $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 75mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	 <p>Schematic diagram</p>  <p>pin assignment</p>  <p>DFN3*3</p>
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Ordering Information

Device	Package	Marking	Packaging
GT700P08D3	DFN3*3	GT700P08	5000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-80	V
Continuous Drain Current	I_D	-16	A
Pulsed Drain Current (note1)	I_{DM}	-64	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	69	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	75	$^\circ\text{C/W}$
Maximum Junction-to-Case	R_{thJC}	1.8	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-80	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -80V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2	-2.5	-3.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -2A$	--	57	75	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -2A$	--	6	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -40V,$ $f = 1.0\text{MHz}$	--	1591	--	pF
Output Capacitance	C_{oss}		--	120	--	
Reverse Transfer Capacitance	C_{rss}		--	5	--	
Total Gate Charge	Q_g	$V_{DD} = -40V,$ $I_D = -10A,$ $V_{GS} = -10V$	--	75	--	nC
Gate-Source Charge	Q_{gs}		--	16	--	
Gate-Drain Charge	Q_{gd}		--	19	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -40V,$ $I_D = -10A,$ $R_G = 3\Omega$	--	18	--	ns
Turn-on Rise Time	t_r		--	20	--	
Turn-off Delay Time	$t_{d(off)}$		--	55	--	
Turn-off Fall Time	t_f		--	35	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-16	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -2A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -20A, V_{GS} = 0V$ $di/dt = -100A/\mu s$	--	71	--	nC
Reverse Recovery Time	T_{rr}		--	49	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical RG

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

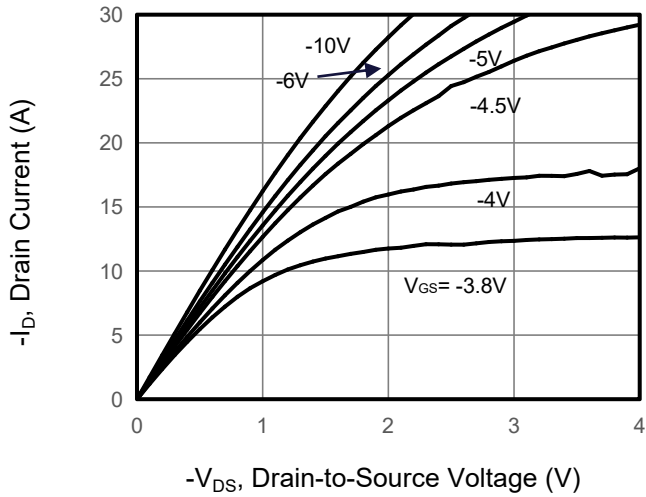


Figure 2. Transfer Characteristics

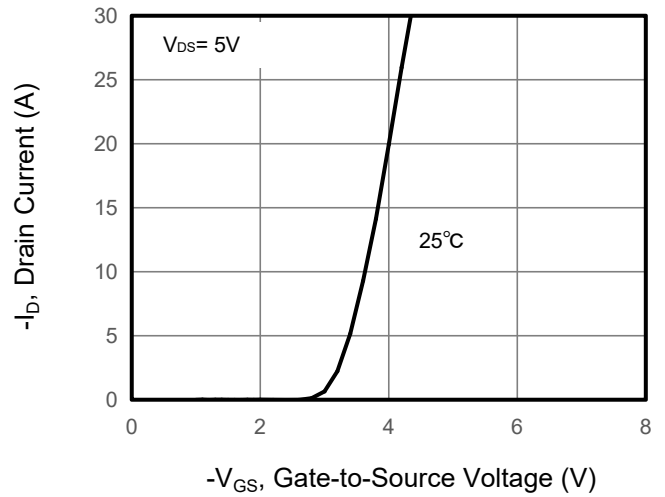


Figure 3. Drain Source On Resistance

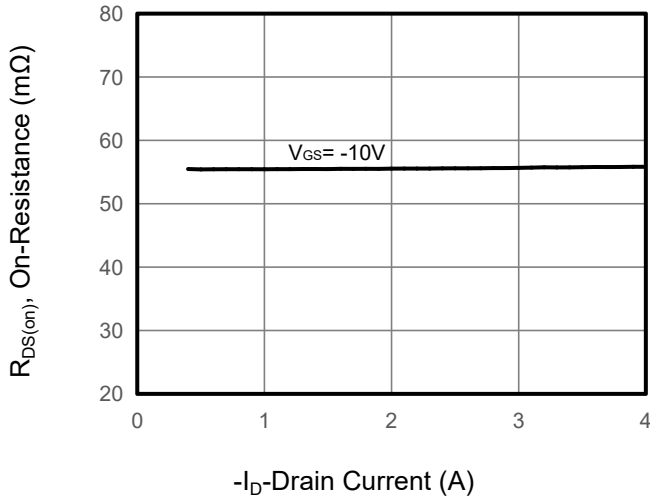


Figure 4. Gate Charge

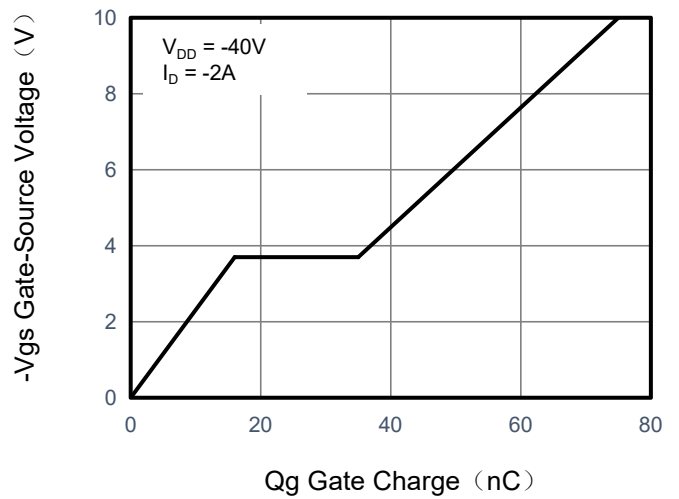


Figure 5. Capacitance

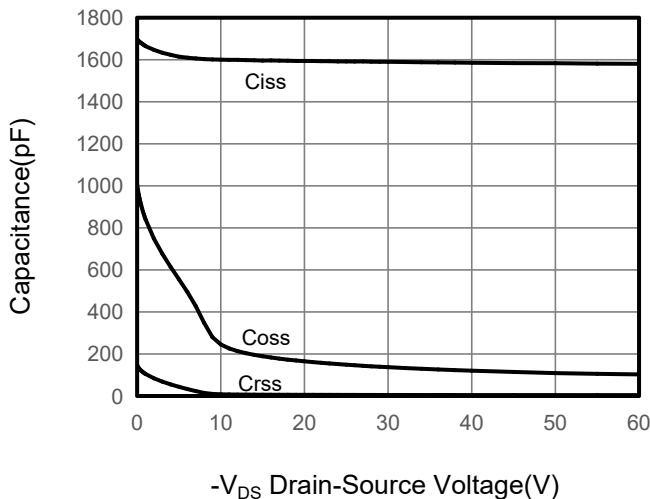
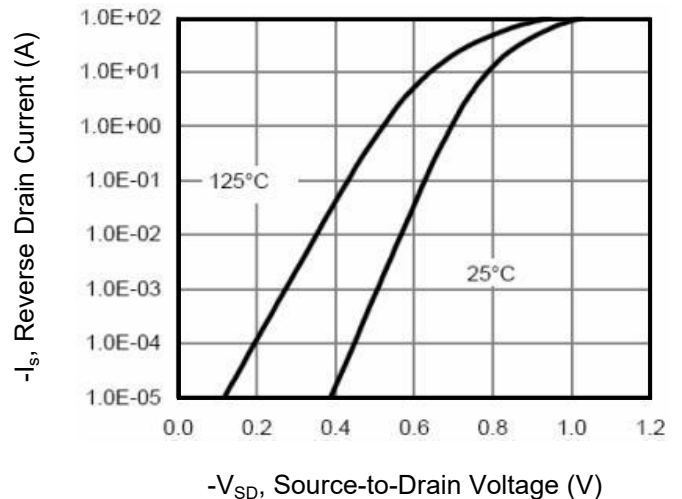


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

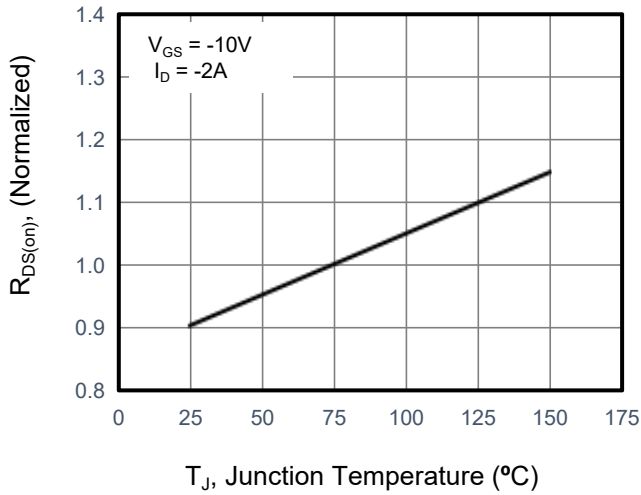


Figure 10. Safe Operation Area

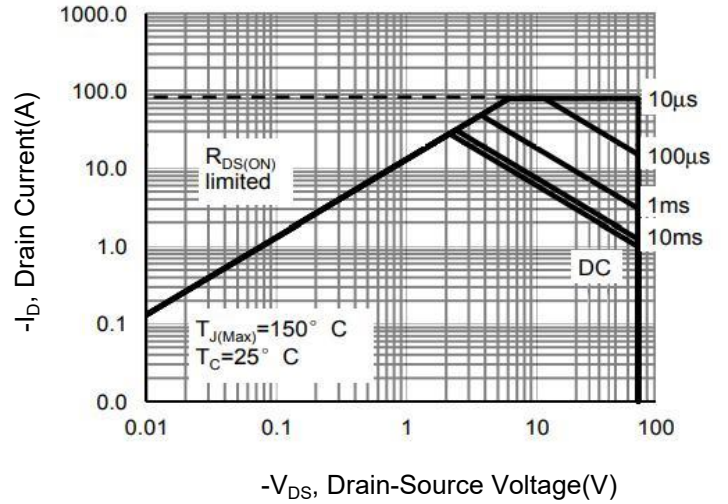
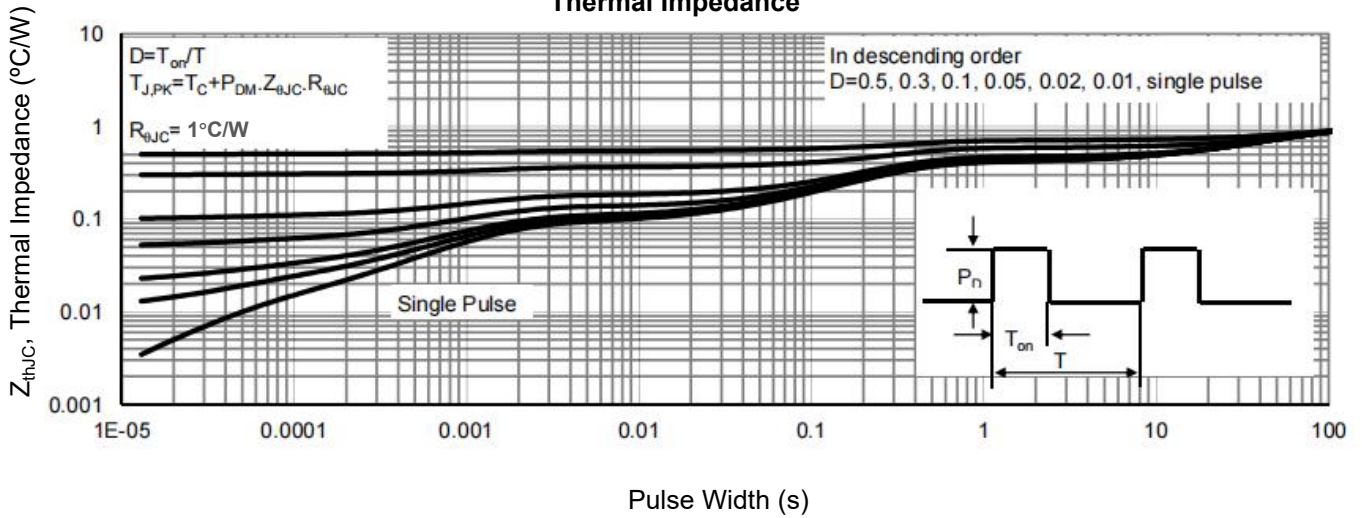
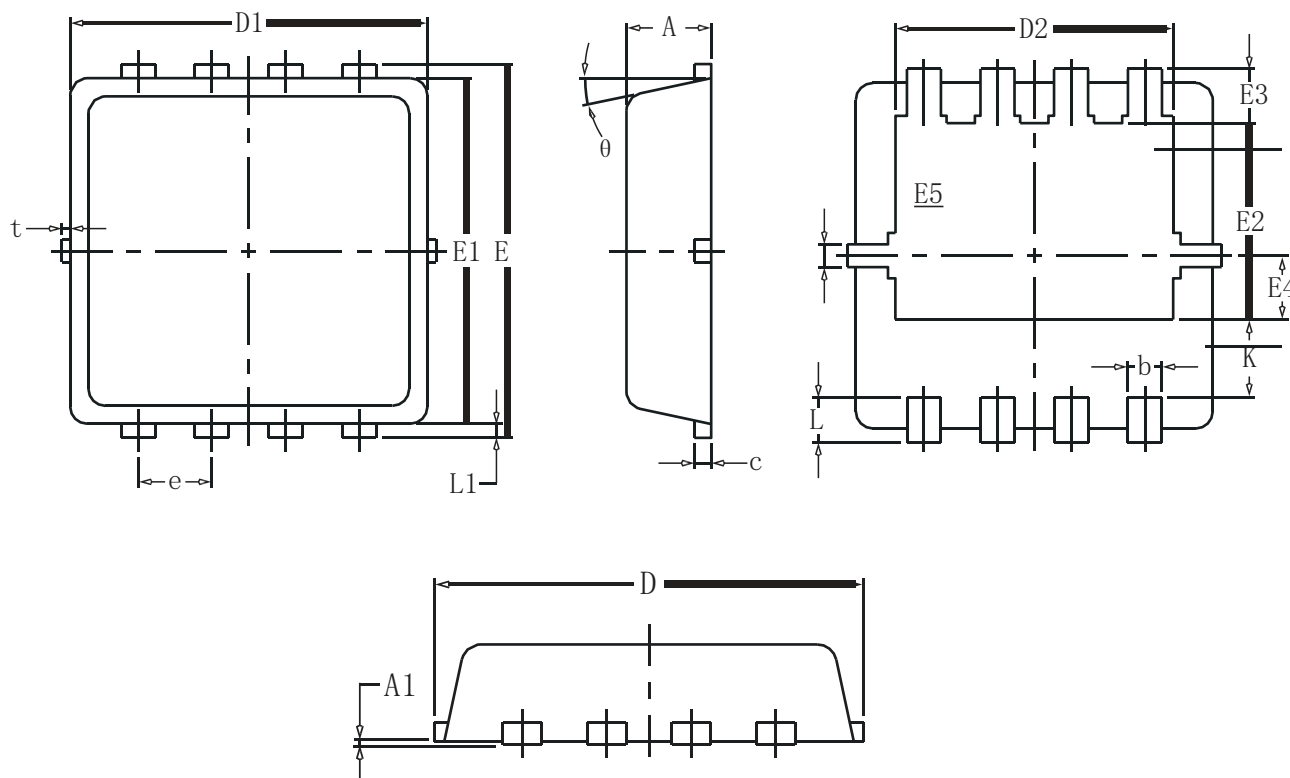


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN3*3 Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°